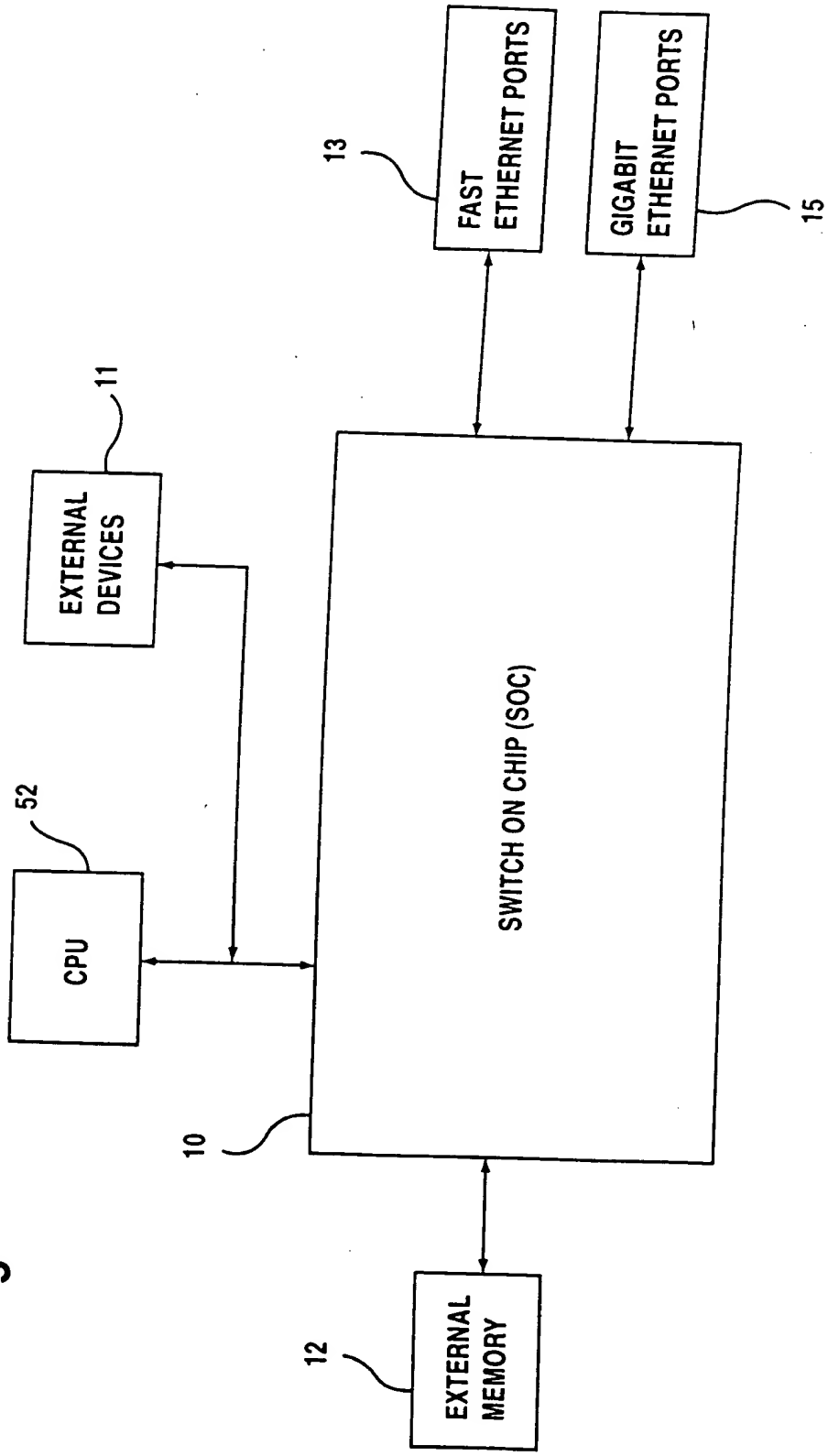

FAST ETHERNET PORTS
13
GIGABIT ETHERNET PORTS
15
EXTERNAL DEVICES
11
SWITCH ON CHIP (SOC)
CPU
52
10
EXTERNAL MEMORY
12

Fig.1

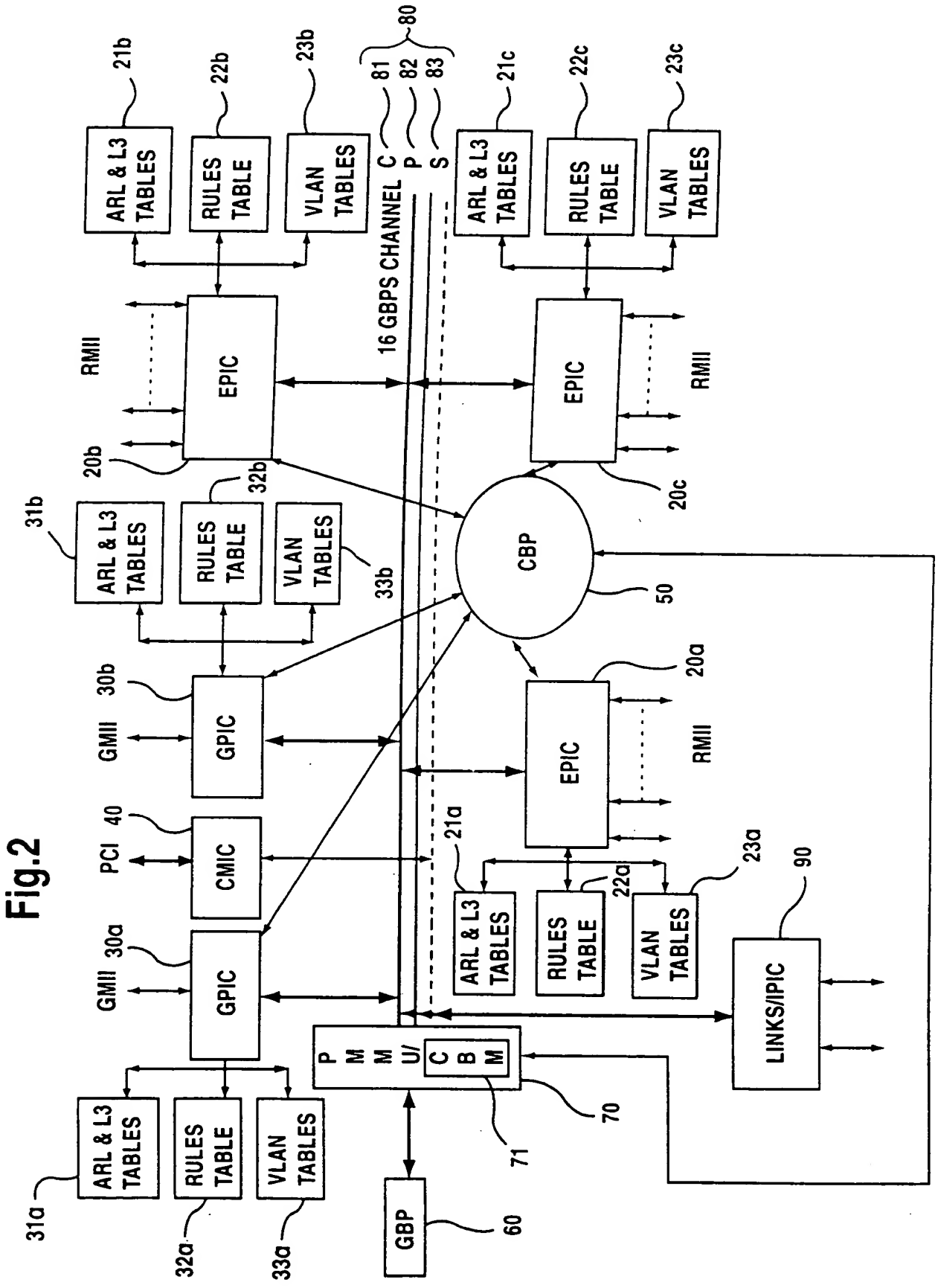
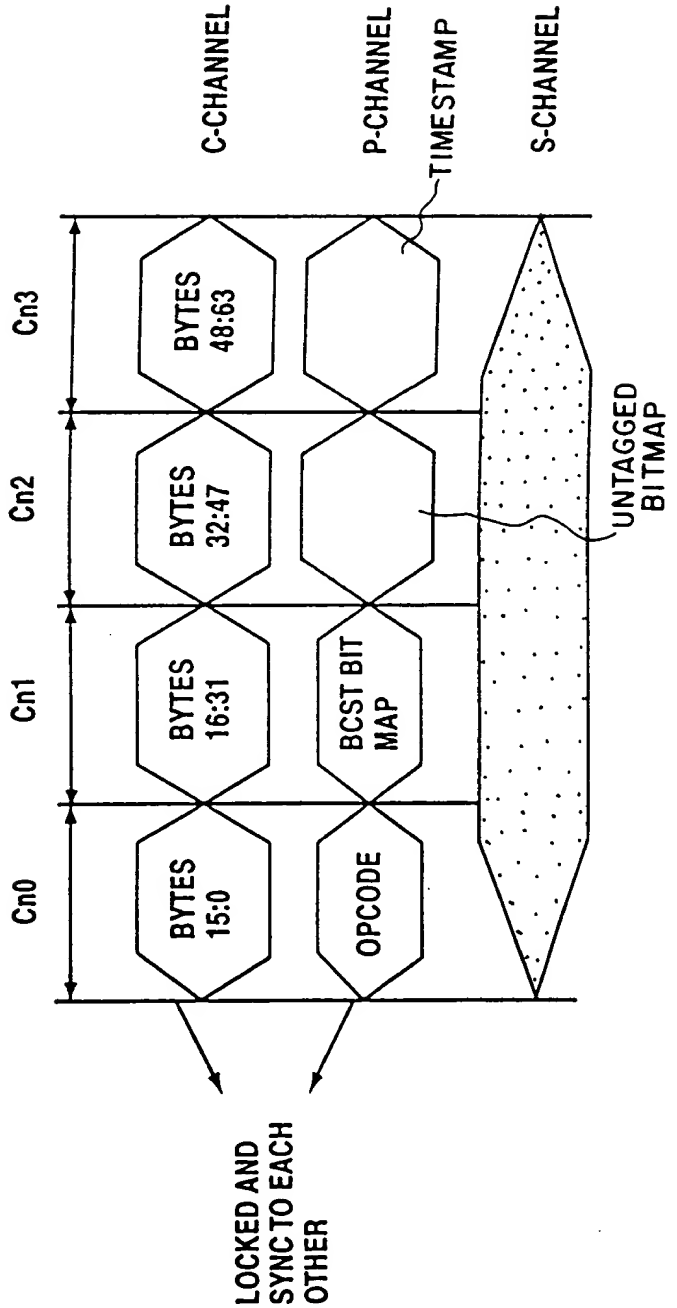

ARL & L3 TABLES
RULES TABLE
VLAN TABLES
21b
22b
23b
80
81
82
83
C
P
S
16 GBPS CHANNEL
21c
22c
23c
RMII
EPIC
20b
20c
32b
31b
33b
CBP
50
30b
GMII
GPIC
20a
PCI
40
CMIC
21a
22a
23a
90
30a
LINKS/IPIC
P M M U/ C B M
70
71
31a
32a
33a
GBP
60

Fig.2

Fig.3


C-CHANNEL
P-CHANNEL
TIMESTAMP
S-CHANNEL
Cn3
Cn2
Cn1
Cn0
BYTES 48:63
BYTES 32:47
BYTES 16:31
BYTES 15:0
BCST BIT MAP
OPCODE
UNTAGGED BITMAP
LOCKED AND SYNC TO EACH OTHER

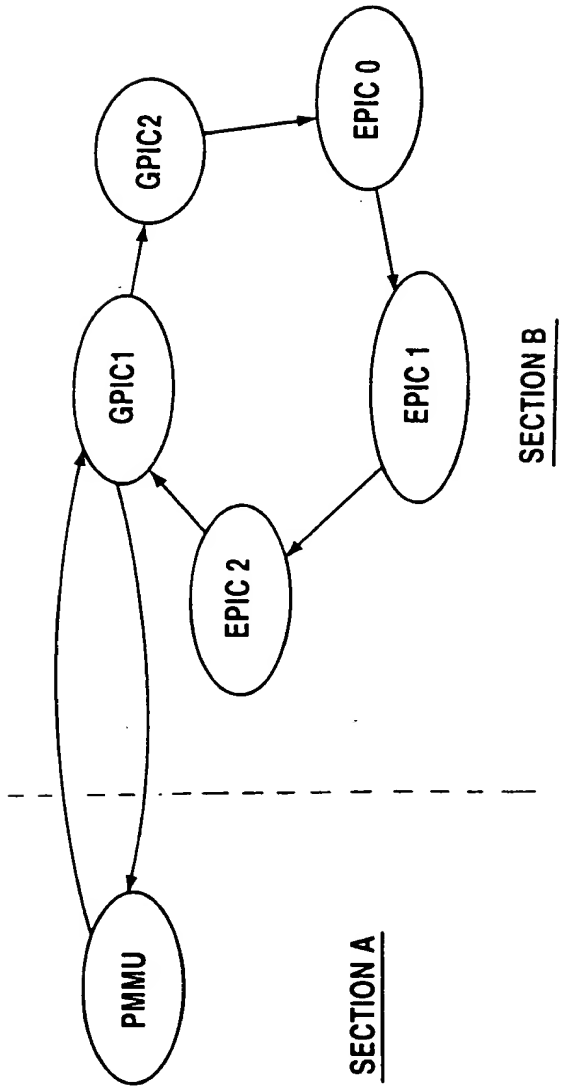

GPIC2
EPIC 0
GPIC1
EPIC 1
EPIC 2
PMMU
SECTION A
SECTION B

Fig.4a

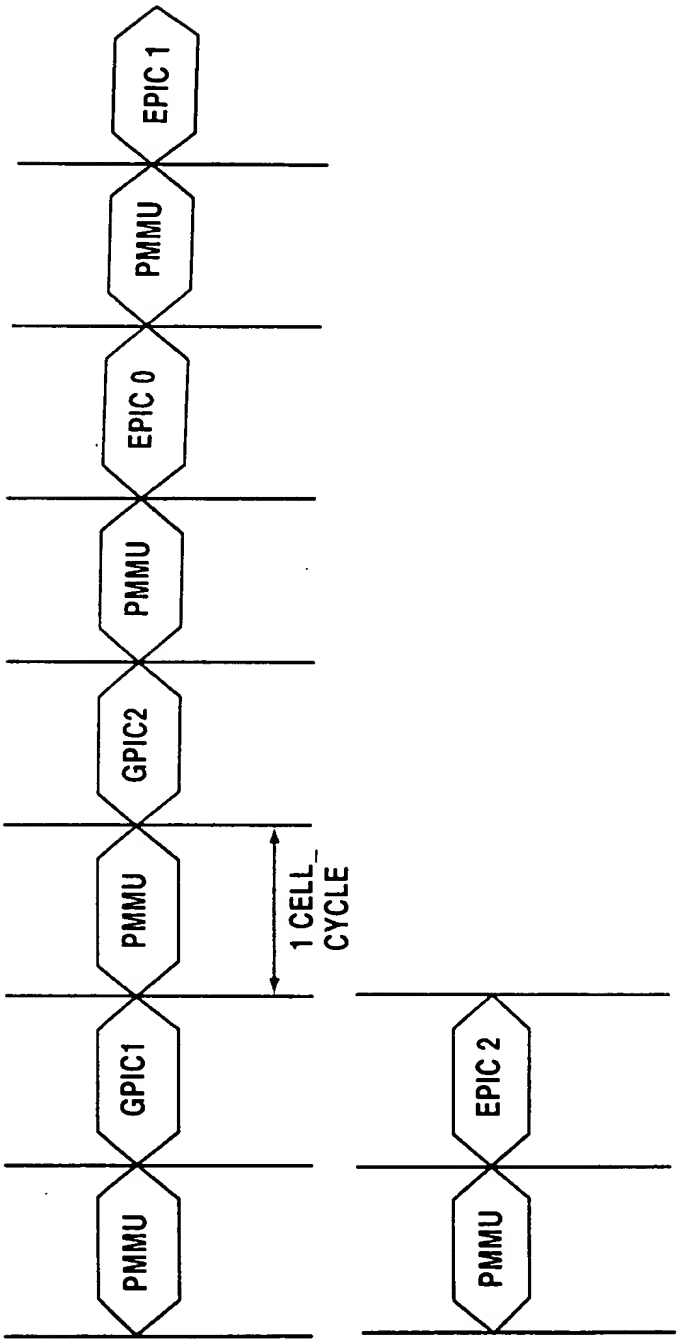

EPIC 1
PMMU
EPIC 0
PMMU
GPIC2
PMMU
GPIC1
PMMU
1 CELL_ CYCLE
EPIC 2
PMMU

Fig.4b

Fig.5

PROTOCOL CHANNEL MESSAGES

30	28		26	24	22	20	18	16	14	12	10	8	6	4	2	0
OP CODE	I P	I P X	RESERVED	NXT CELL	SRC DEST PORT			COS	J	S	E	CR C	P	O	LEN	

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
RESERVED	BC/MC PORTBITMAP														

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	RES	UNTAGGED PORTBITMAP/SRC PORT NUMBER (BIT0..5)													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
CPU OPCODES									TIME STAMP						

Fig.6

SIDE BAND CHANNEL MESSAGES

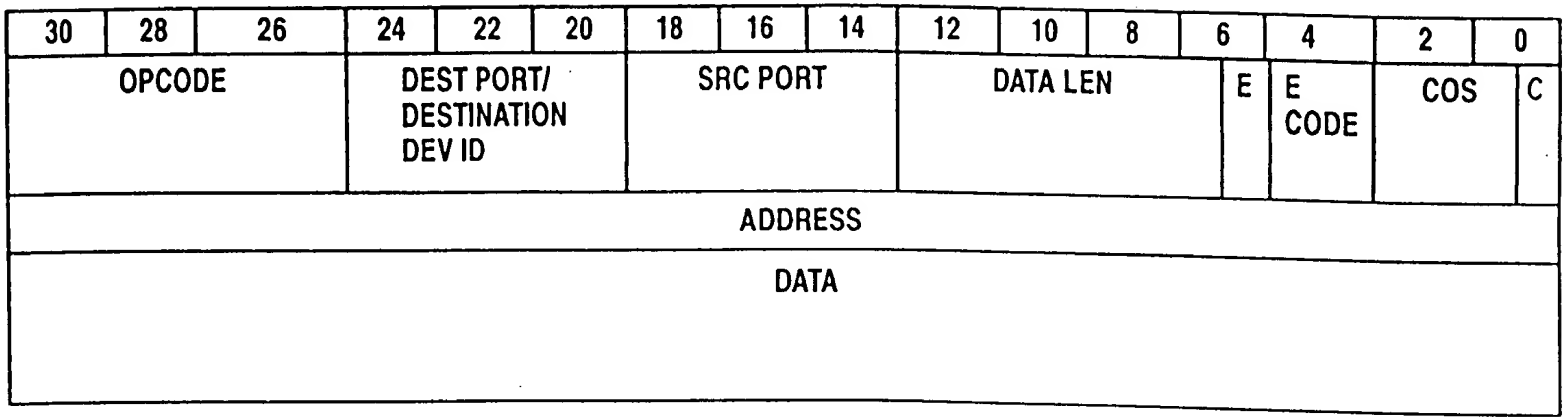
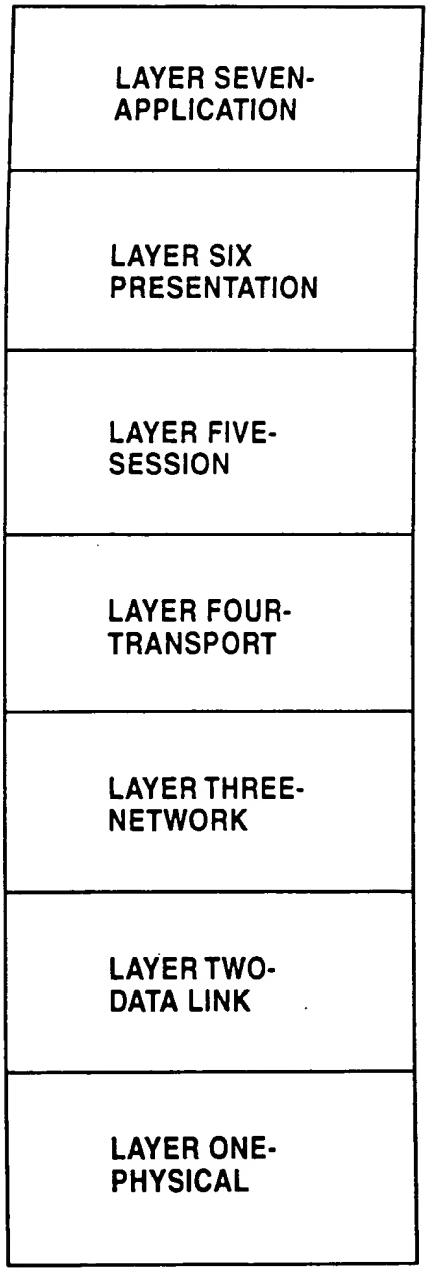


Fig.7
PRIOR ART



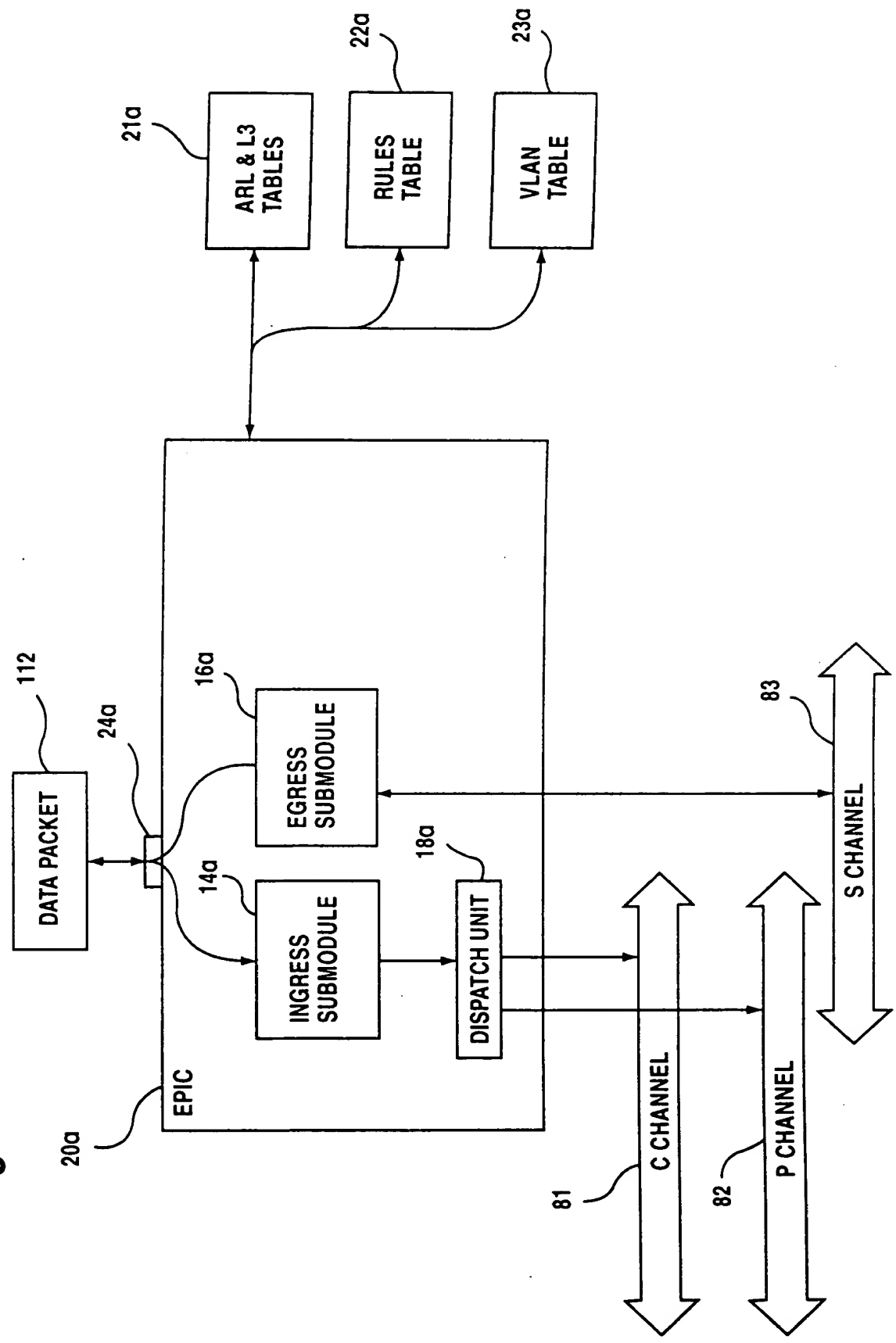

21a
ARL & L3 TABLES
22a
RULES TABLE
23a
VLAN TABLE
112
DATA PACKET
24a
16a
EGRESS SUBMODULE
14a
INGRESS SUBMODULE
18a
DISPATCH UNIT
EPIC
20a
83
S CHANNEL
81
C CHANNEL
82
P CHANNEL

Fig.8

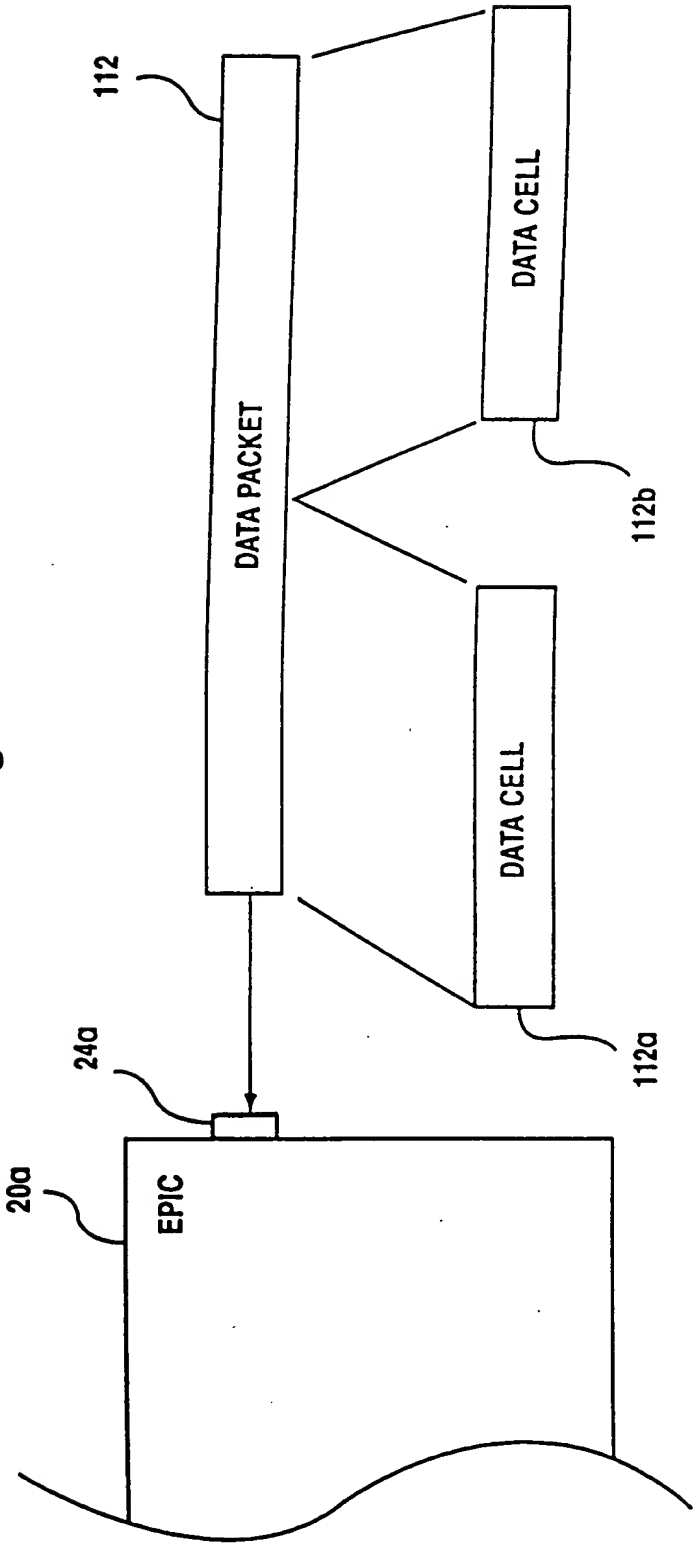


Fig.9

Fig.10

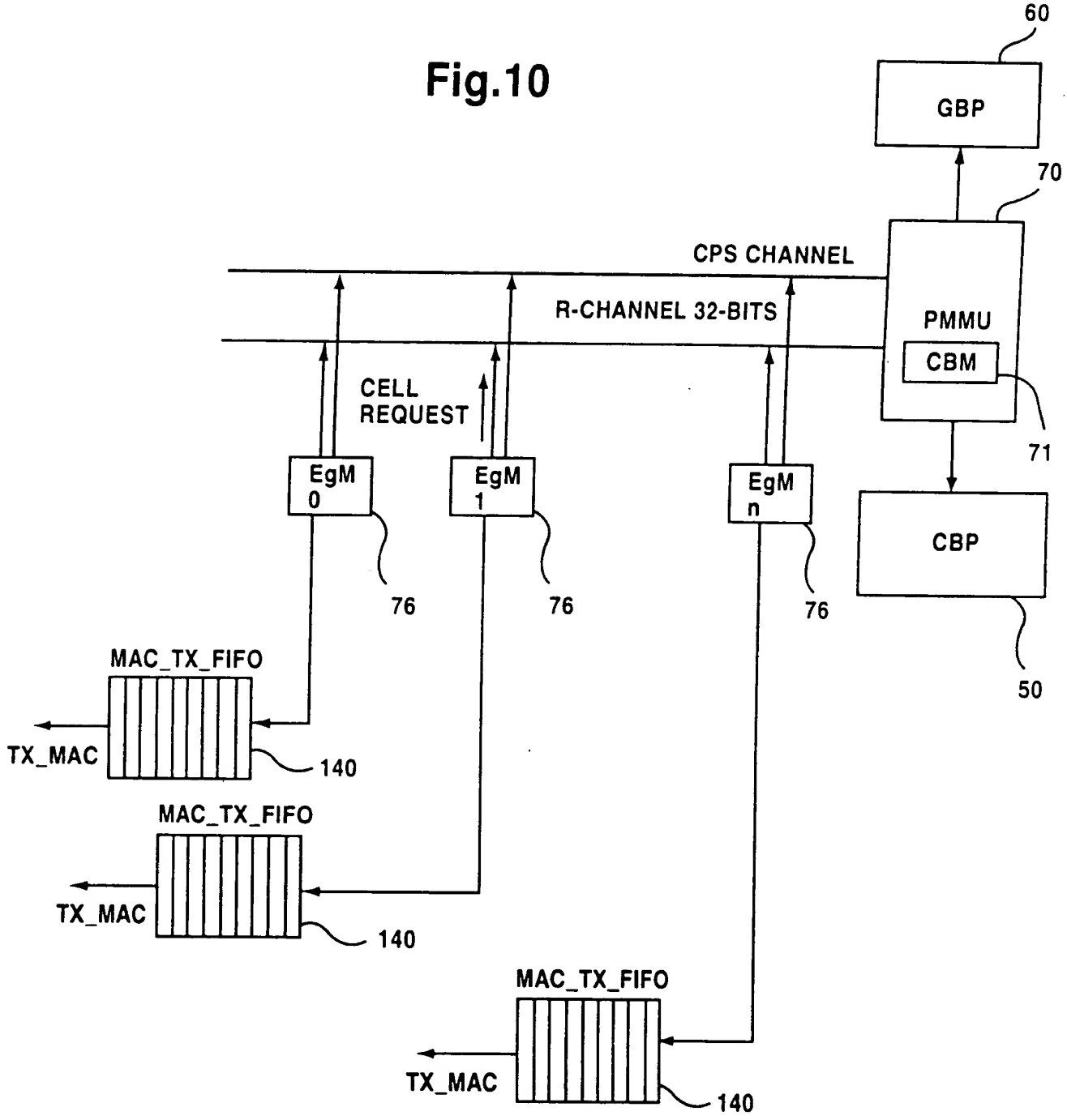

60
GBP
70
CPS CHANNEL
R-CHANNEL 32-BITS
PMMU
CBM
71
CELL
REQUEST
EgM
0
EgM
1
EgM
n
76
76
76
CBP
50
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140

Fig.11

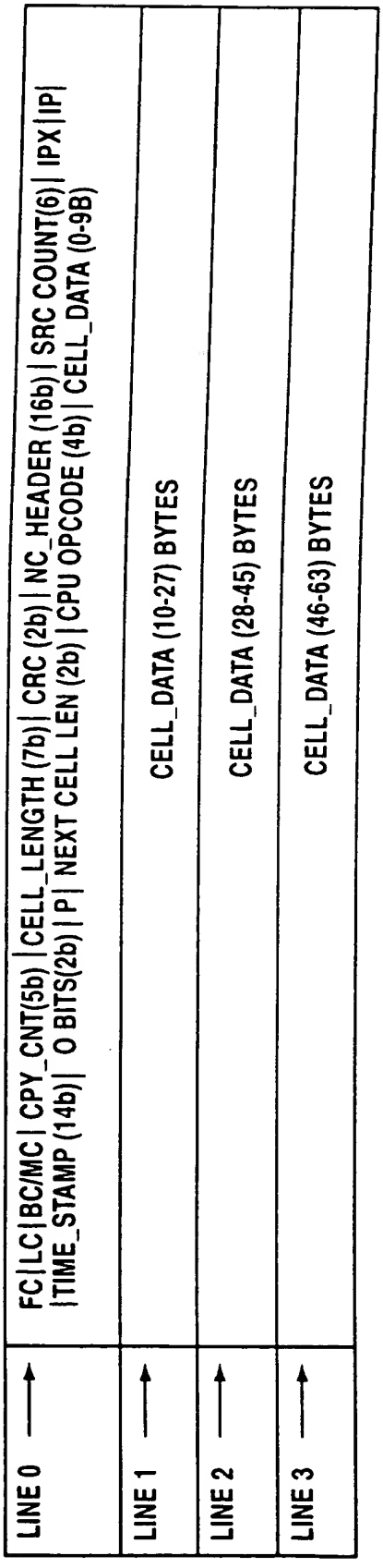

LINE 0
FC|LC|BC/MC| CPY_CNT(5b) |CELL_LENGTH (7b)| CRC (2b)| NC_HEADER (16b)| SRC COUNT(6)| IPX|IP|
|TIME_STAMP (14b)| O BITS(2b) | P| NEXT CELL LEN (2b) | CPU OPCODE (4b)| CELL_DATA (0-9B)
LINE 1
CELL_DATA (10-27) BYTES
LINE 2
CELL_DATA (28-45) BYTES
LINE 3
CELL_DATA (46-63) BYTES

Fig.12

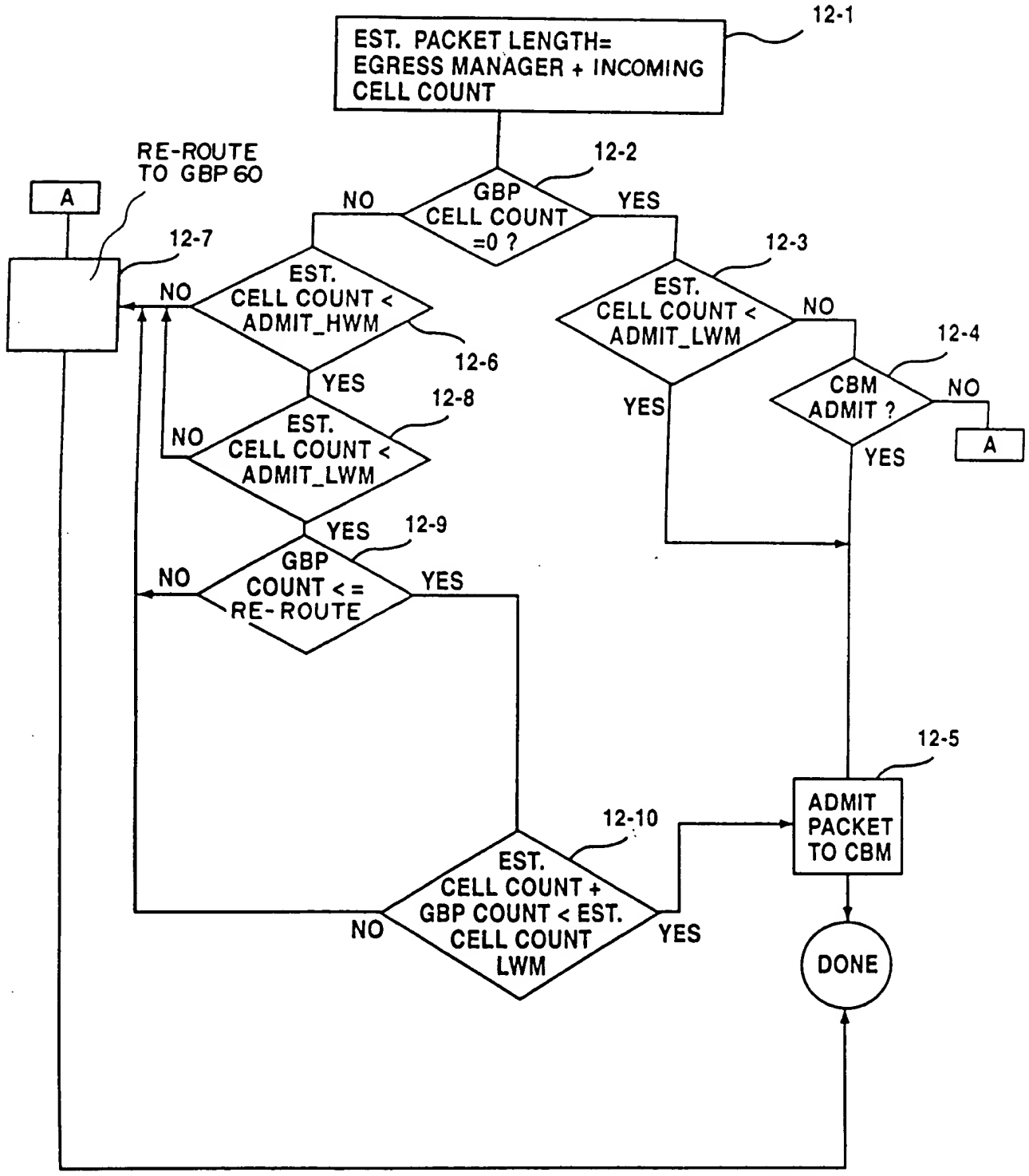

EST. PACKET LENGTH= EGRESS MANAGER + INCOMING CELL COUNT
12-1
GBP CELL COUNT =0 ?
12-2
NO
YES
EST. CELL COUNT < ADMIT_LWM
12-3
NO
YES
CBM ADMIT ?
12-4
NO
YES
A
RE-ROUTE TO GBP 60
A
12-7
NO
EST. CELL COUNT < ADMIT_HWM
12-6
YES
NO
EST. CELL COUNT < ADMIT_LWM
12-8
YES
GBP COUNT < = RE-ROUTE
12-9
NO
YES
ADMIT PACKET TO CBM
12-5
EST. CELL COUNT + GBP COUNT < EST. CELL COUNT LWM
12-10
NO
YES
DONE

Fig.13

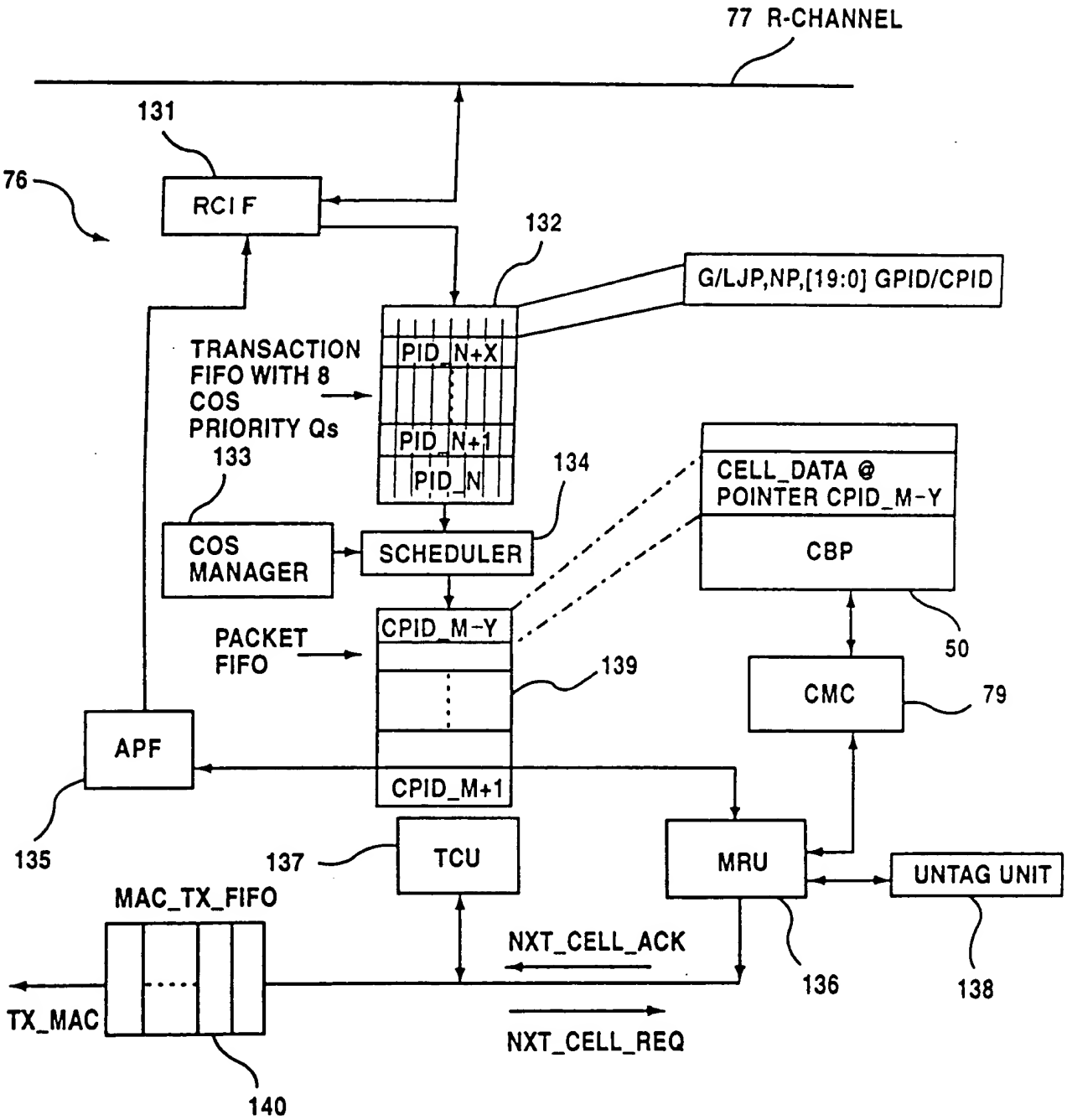

77 R-CHANNEL
131
76
RCI F
132
G/LJP,NP,[19:0] GPID/CPID
TRANSACTION FIFO WITH 8 COS PRIORITY Qs
PID_N+X
PID_N+1
PID_N
133
134
CELL_DATA @ POINTER CPID_M-Y
CBP
COS MANAGER
SCHEDULER
CPID_M-Y
PACKET FIFO
139
50
CMC
79
APF
CPID_M+1
135
137
TCU
MRU
UNTAG UNIT
MAC_TX_FIFO
NXT_CELL_ACK
136
138
TX_MAC
NXT_CELL_REQ
140

Fig.14

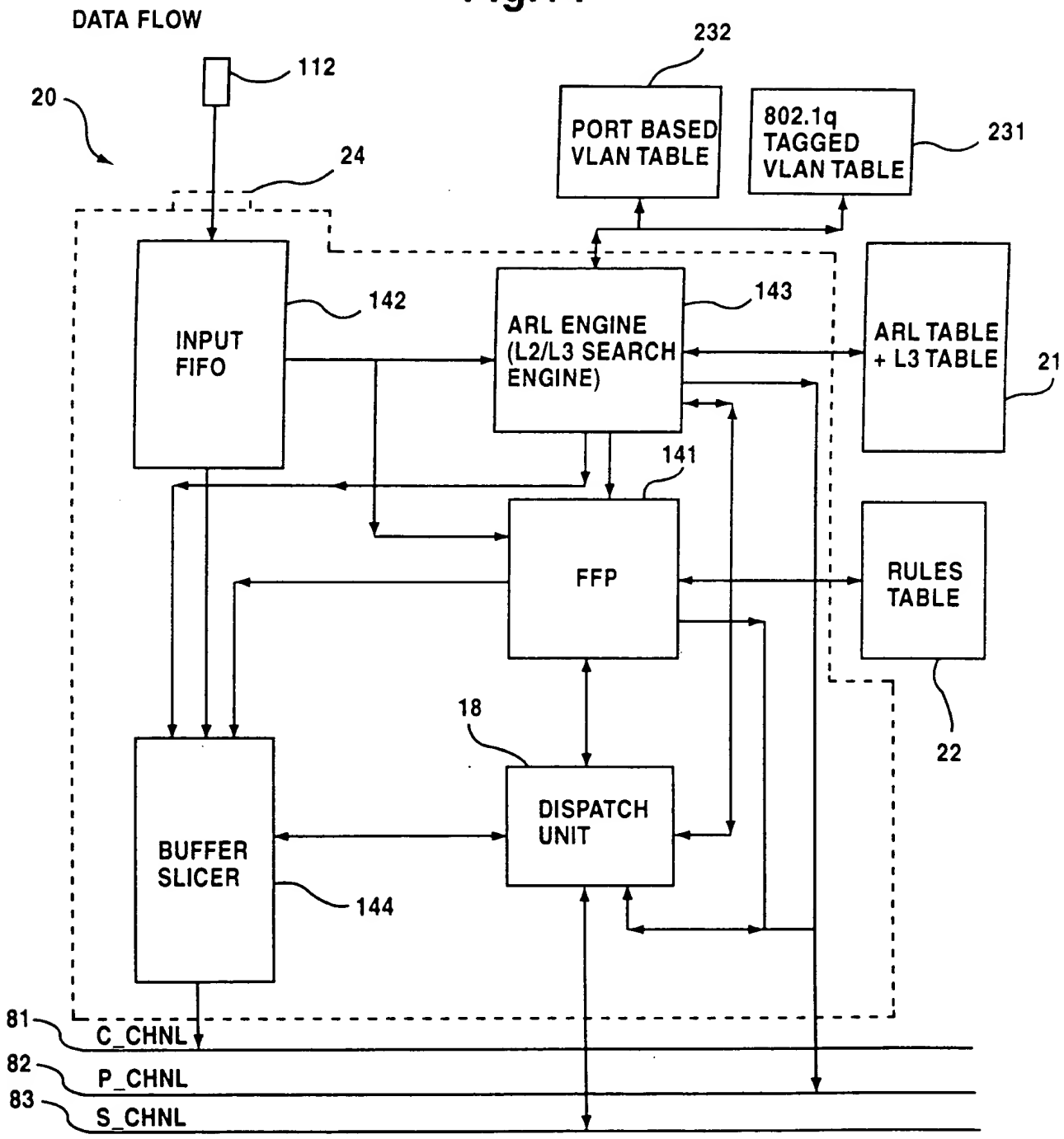

DATA FLOW
20
112
24
232
PORT BASED VLAN TABLE
802.1q TAGGED VLAN TABLE
231
INPUT FIFO
142
ARL ENGINE (L2/L3 SEARCH ENGINE)
143
ARL TABLE + L3 TABLE
21
141
FFP
RULES TABLE
22
18
DISPATCH UNIT
BUFFER SLICER
144
81
C_CHNL
82
P_CHNL
83
S_CHNL

Fig.15

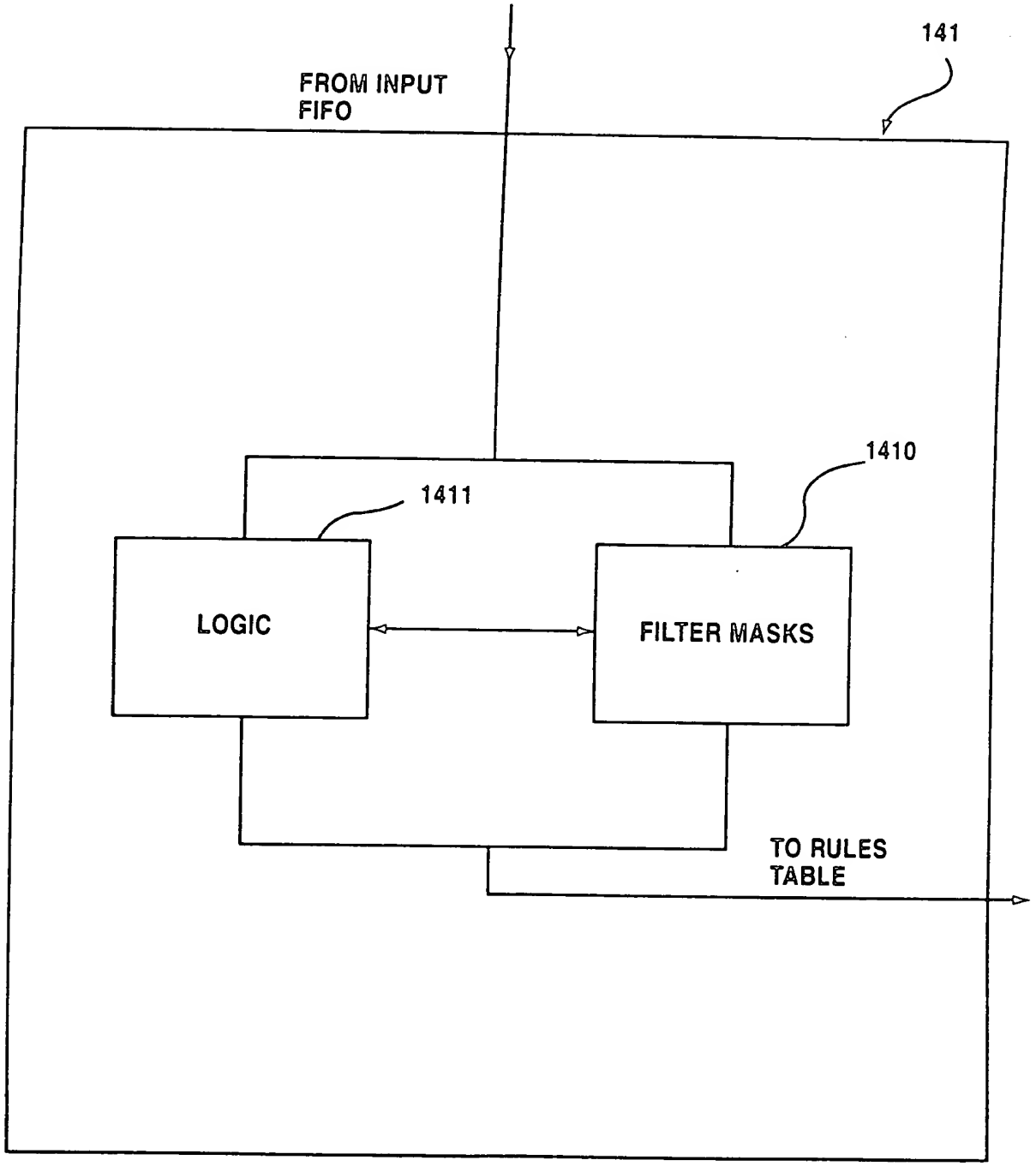

141
FROM INPUT FIFO
1410
1411
LOGIC
FILTER MASKS
TO RULES TABLE

Fig.16

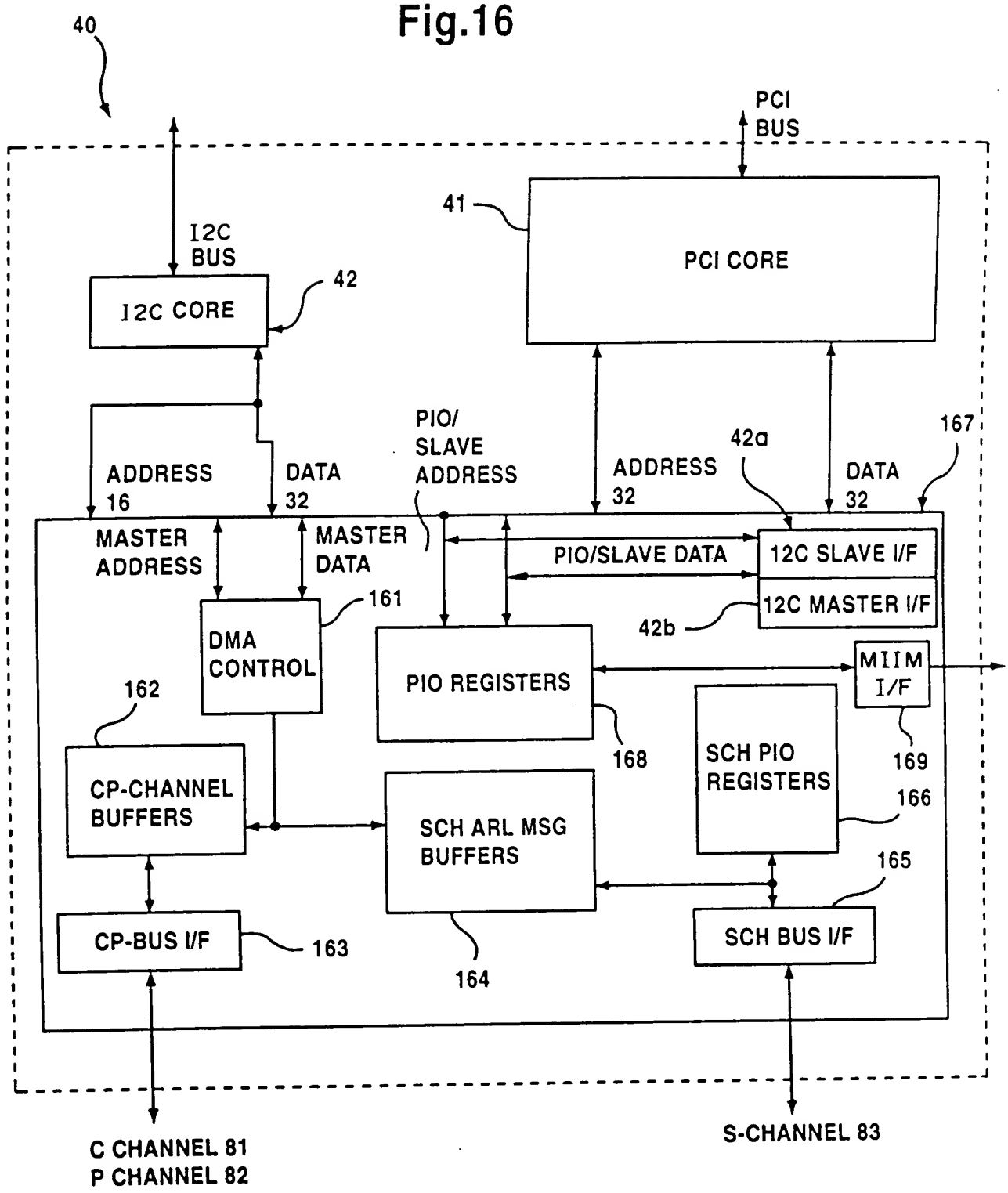

40
PCI BUS
41
PCI CORE
I2C BUS
I2C CORE
42
ADDRESS 16
DATA 32
PIO/ SLAVE ADDRESS
ADDRESS 32
42a
DATA 32
167
MASTER ADDRESS
MASTER DATA
PIO/SLAVE DATA
12C SLAVE I/F
12C MASTER I/F
42b
161
DMA CONTROL
PIO REGISTERS
MIIM I/F
162
168
169
SCH PIO REGISTERS
166
CP-CHANNEL BUFFERS
SCH ARL MSG BUFFERS
165
CP-BUS I/F
163
164
SCH BUS I/F
C CHANNEL 81
P CHANNEL 82
S-CHANNEL 83

Fig.17

FFP PROGRAMMING FLOW CHART

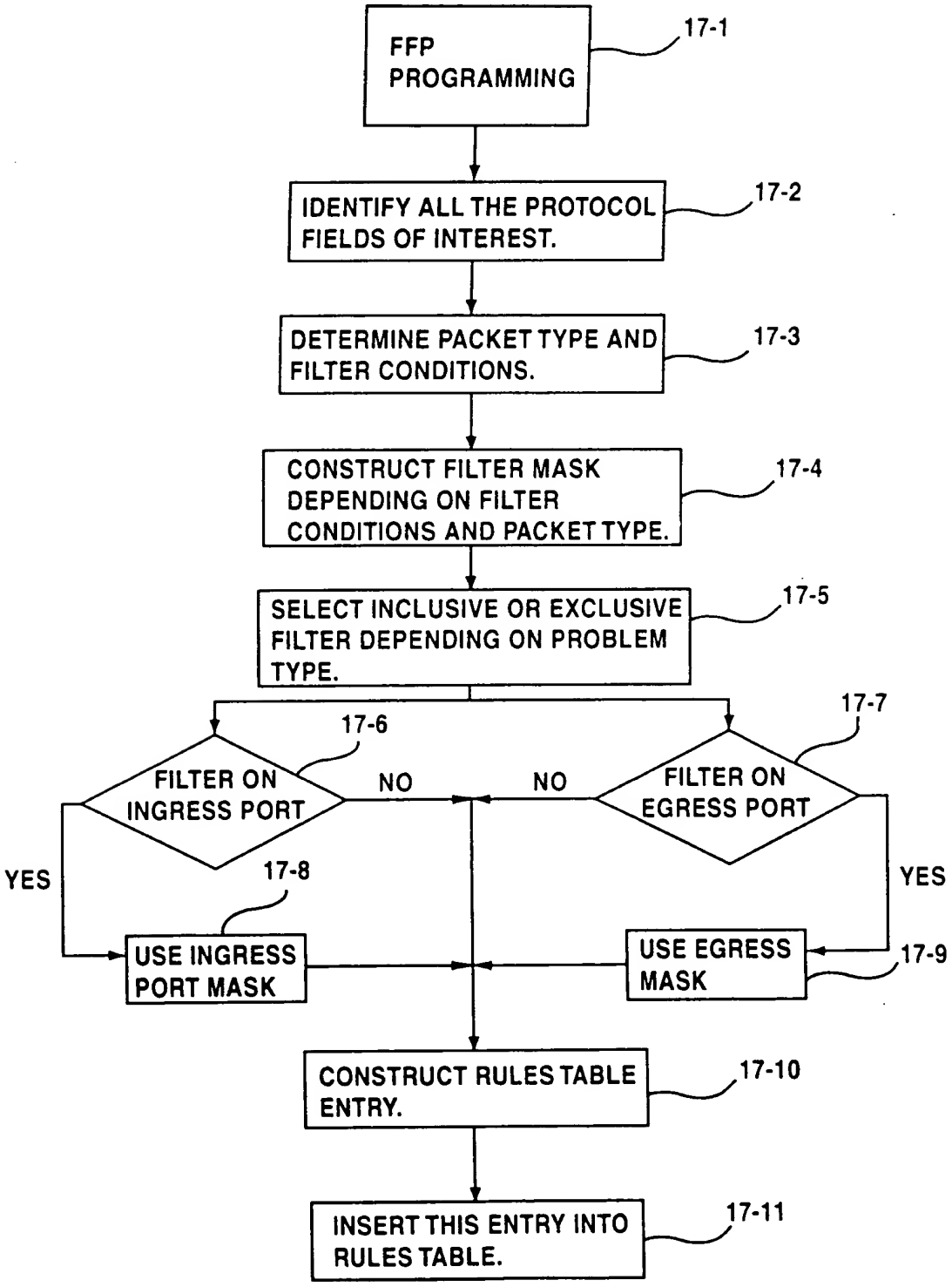


Fig.18

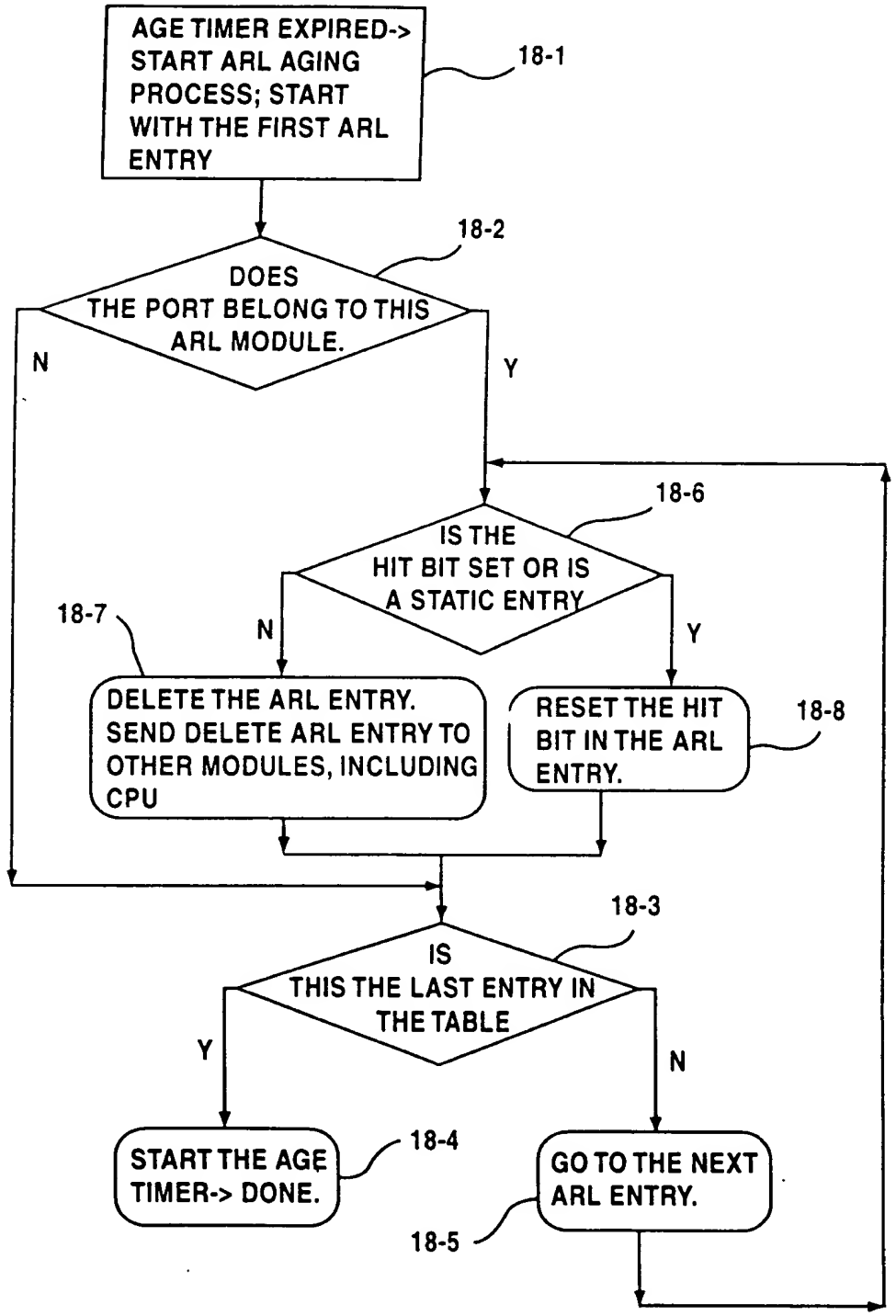
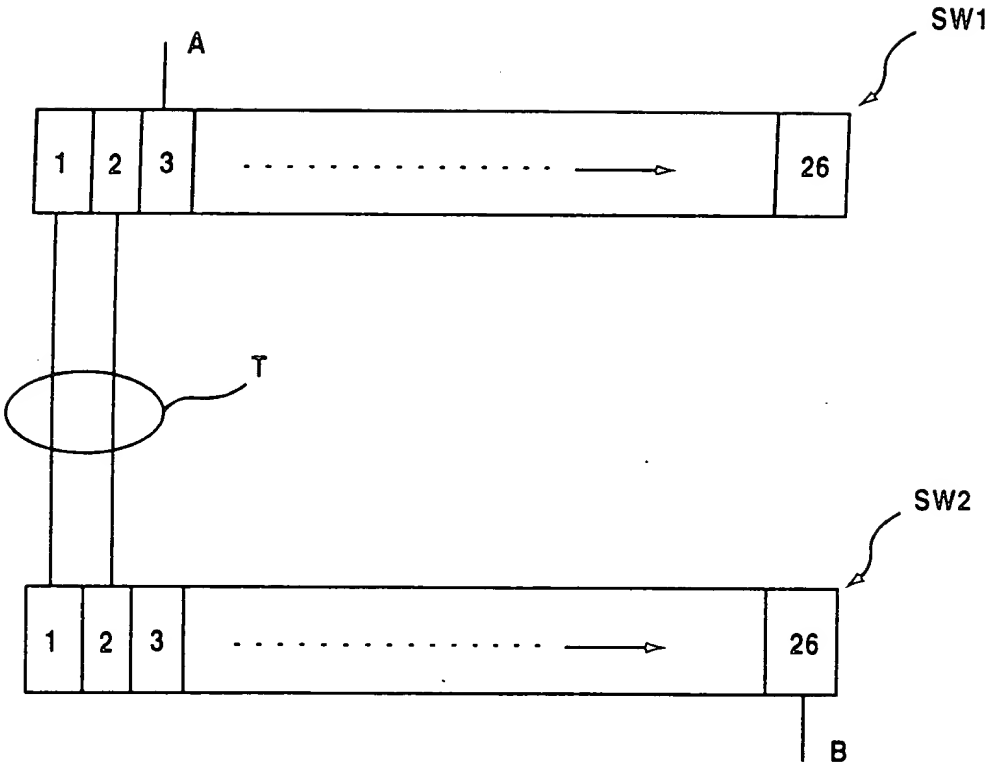

AGE TIMER EXPIRED-> START ARL AGING PROCESS; START WITH THE FIRST ARL ENTRY
18-1
18-2
DOES THE PORT BELONG TO THIS ARL MODULE.
N
Y
18-6
IS THE HIT BIT SET OR IS A STATIC ENTRY
18-7
N
Y
DELETE THE ARL ENTRY. SEND DELETE ARL ENTRY TO OTHER MODULES, INCLUDING CPU
RESET THE HIT BIT IN THE ARL ENTRY.
18-8
18-3
IS THIS THE LAST ENTRY IN THE TABLE
Y
N
START THE AGE TIMER-> DONE.
18-4
GO TO THE NEXT ARL ENTRY.
18-5

Fig.19



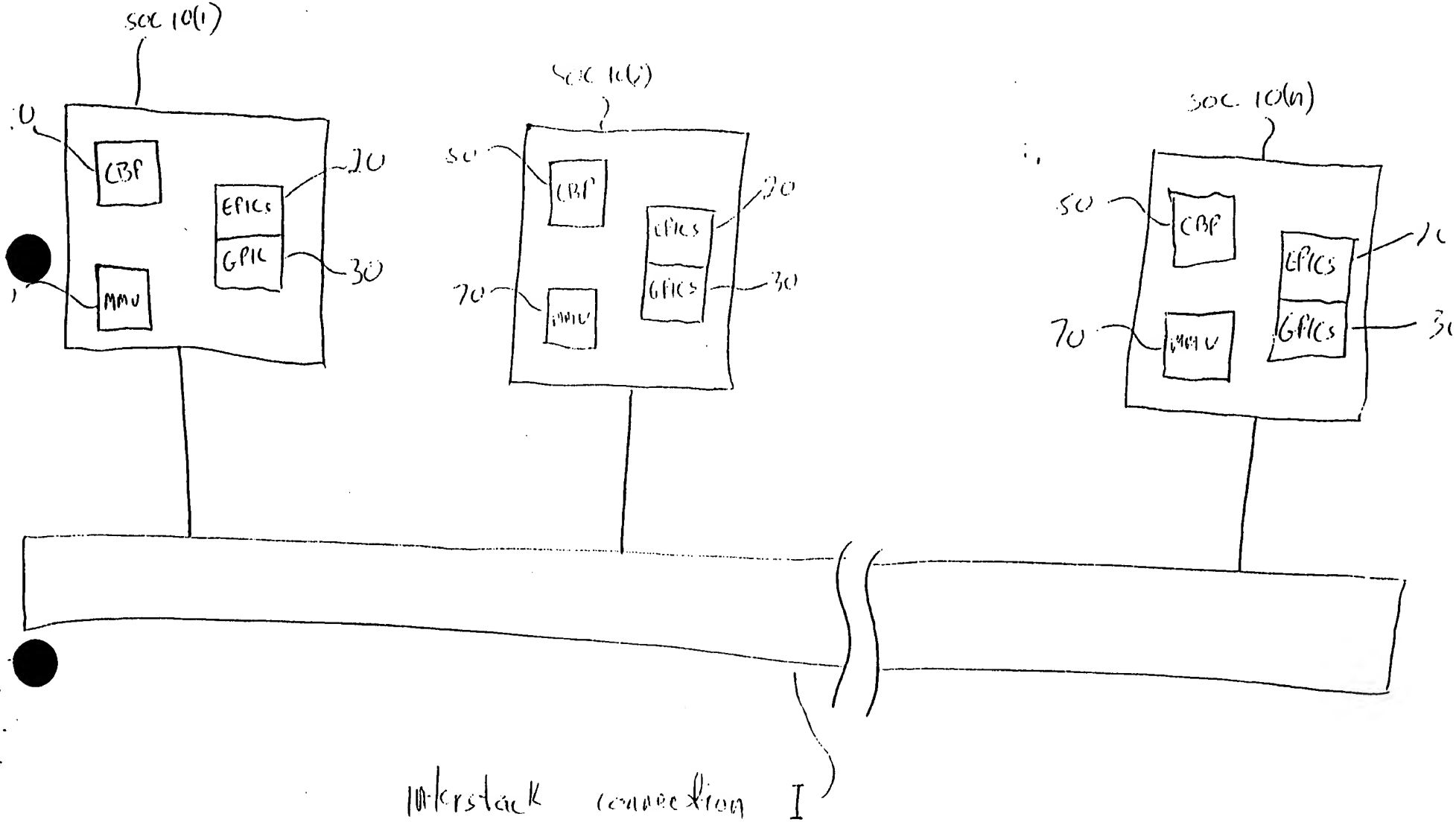

SOC 10(1)
SOC 10(2)
SOC 10(n)
CBP
EPICS
GPIC
MMU
Interstack connection I

Fig 20

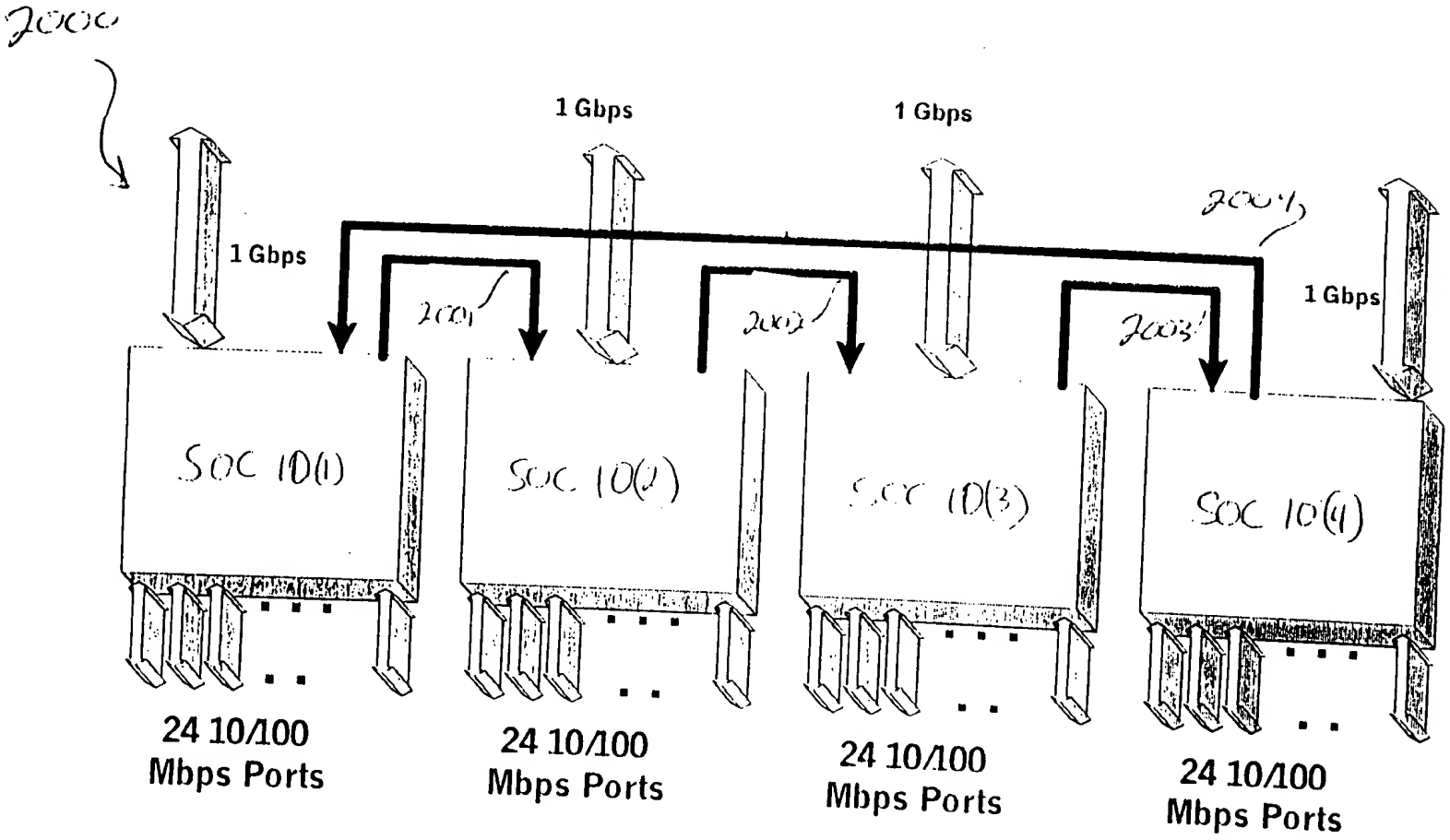

2000
1 Gbps
1 Gbps
1 Gbps
2004
2001
2002
2003
1 Gbps
SOC 10(1)
SOC 10(2)
SOC 10(3)
SOC 10(4)
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports

Fig. 21

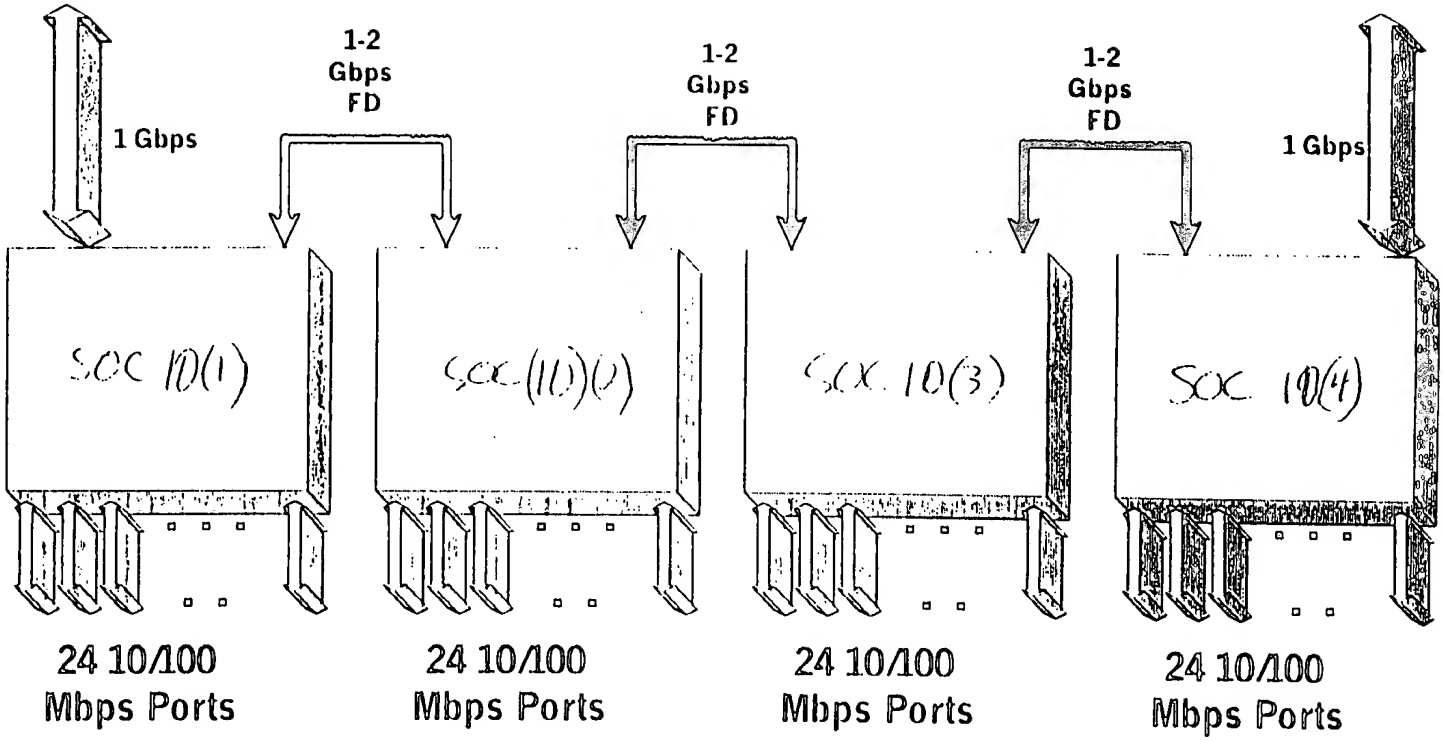

1 Gbps
1-2 Gbps FD
1-2 Gbps FD
1-2 Gbps FD
1 Gbps
SOC 10(1)
SOC (10)(2)
SOC 10(3)
SOC 10(4)
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports

Fig. 22

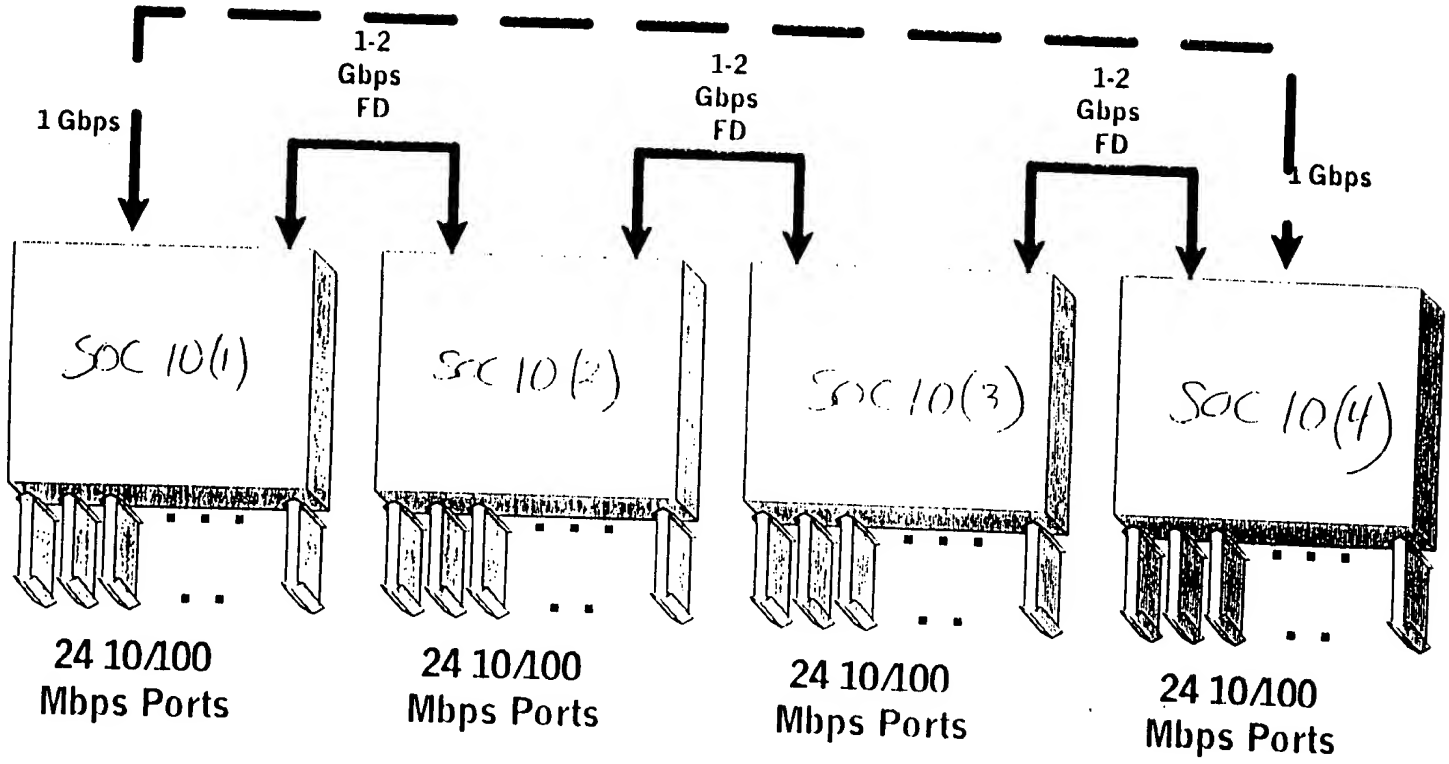

1 Gbps
1-2 Gbps FD
1-2 Gbps FD
1-2 Gbps FD
1 Gbps
SOC 10(1)
SOC 10(2)
SOC 10(3)
SOC 10(4)
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports

Fig. 23

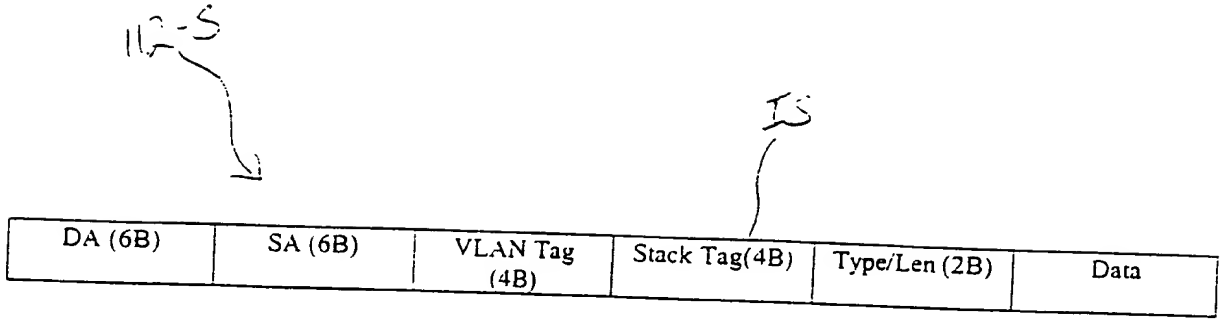


Fig. 24A

IS

Stack Count (5b)	SRC_T (1b)	SRC_TGID (3b)	SRC_RTAG (3b)	DST_T (1b)	DST_TGID (3b)	DST_RTAG (3b)	PFM (2b)	M (1b)	MD (1b)	Res (9)

Fig. 24B

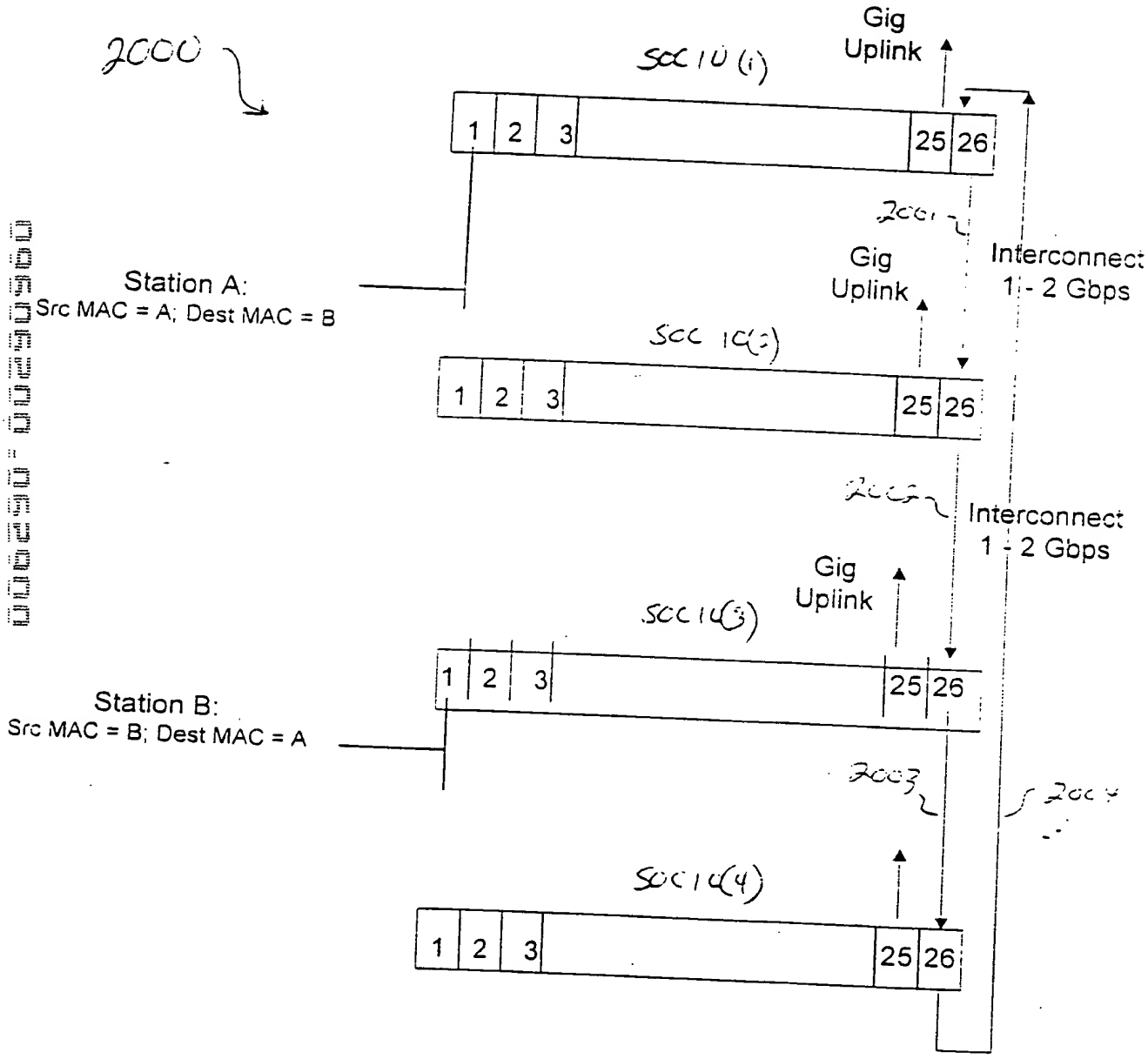

2000
SCC 10 (1)
Gig Uplink
1
2
3
25
26
2001
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
Gig Uplink
SCC 10(2)
2002
Interconnect 1 - 2 Gbps
Gig Uplink
SCC 10(3)
Station B:
Src MAC = B; Dest MAC = A
2003
2004
SCC 10(4)

Fig 25

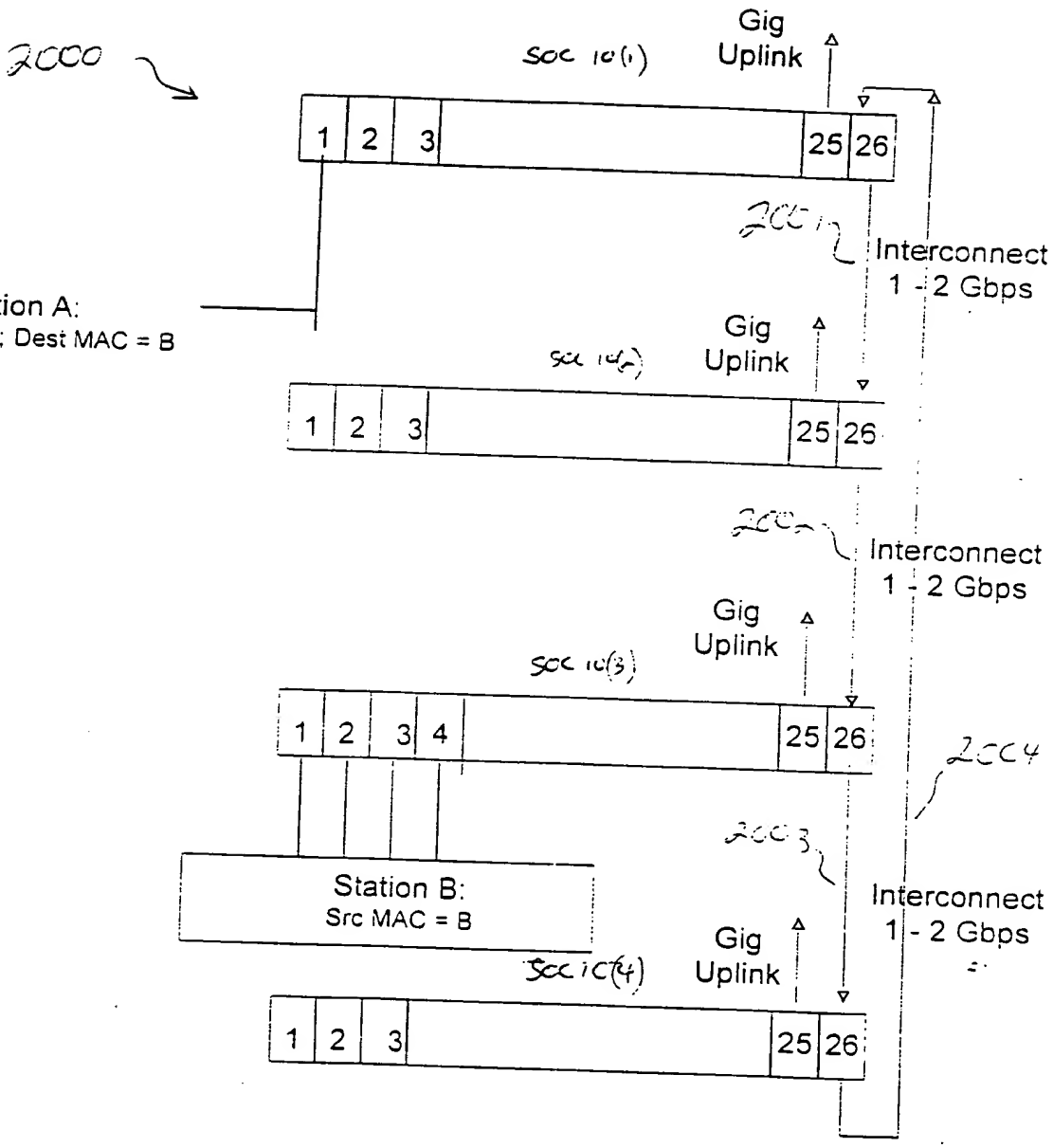

2000
SOC 10(1)
Gig Uplink
1
2
3
25
26
2001
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
SOC 10(2)
Gig Uplink
2002
Interconnect 1 - 2 Gbps
Gig Uplink
SOC 10(3)
4
2004
2003
Station B:
Src MAC = B
Interconnect 1 - 2 Gbps
SOC 10(4)
Gig Uplink

Fig 26

Fig. 27A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	0	X	X
26	B	1	1	2	2

Fig. 27B

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
26	B	1	1	2	2

Fig. 27C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig. 27D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
26	B	1	1	2	2

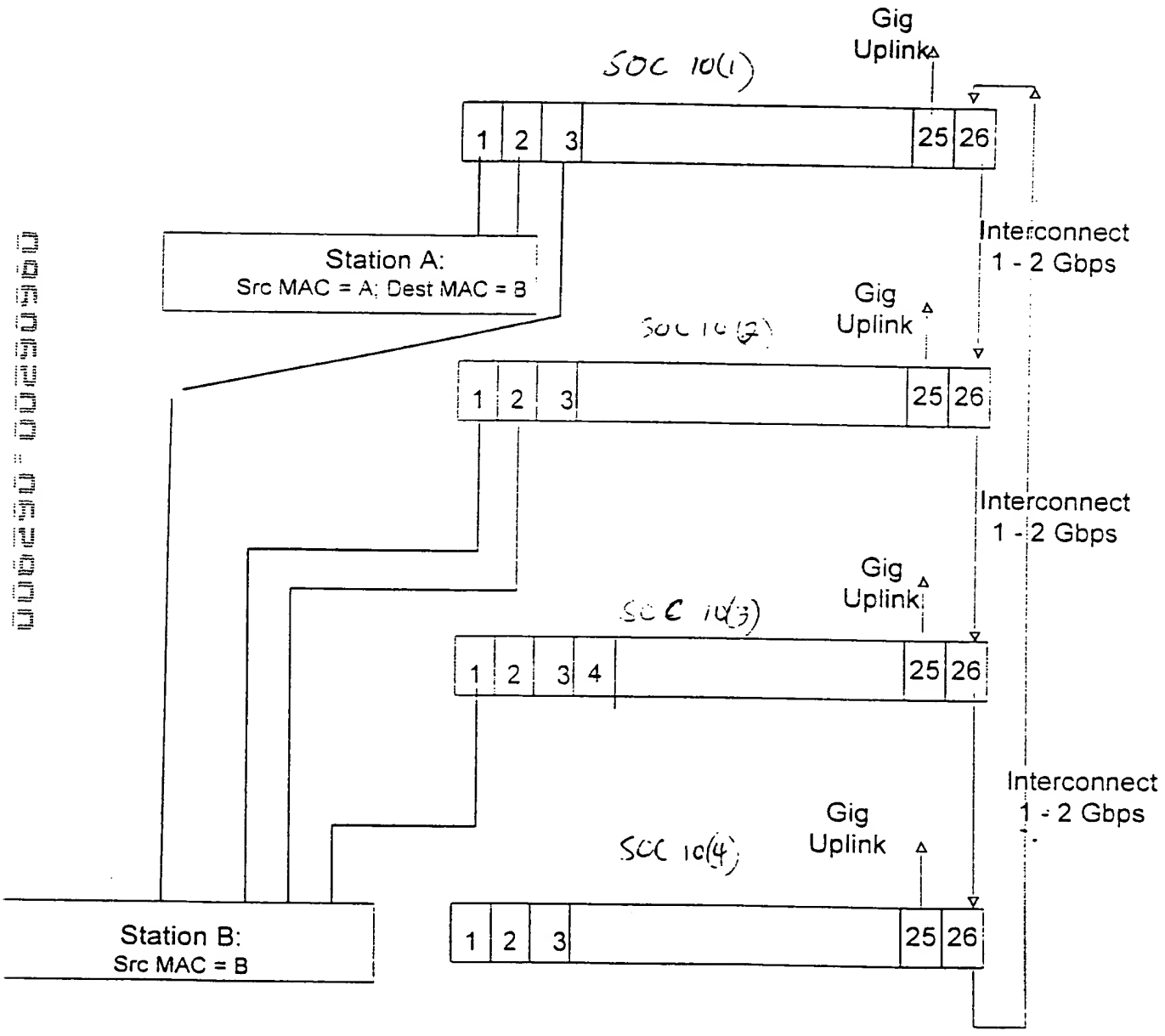

SOC 10(1)
Gig Uplink
1
2
3
25
26
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
SOC 10(2)
Gig Uplink
1
2
3
25
26
Interconnect 1 - 2 Gbps
SOC 10(3)
Gig Uplink
1
2
3
4
25
26
Interconnect 1 - 2 Gbps
SOC 10(4)
Gig Uplink
1
2
3
25
26
Station B:
Src MAC = B

Fig. 3 8

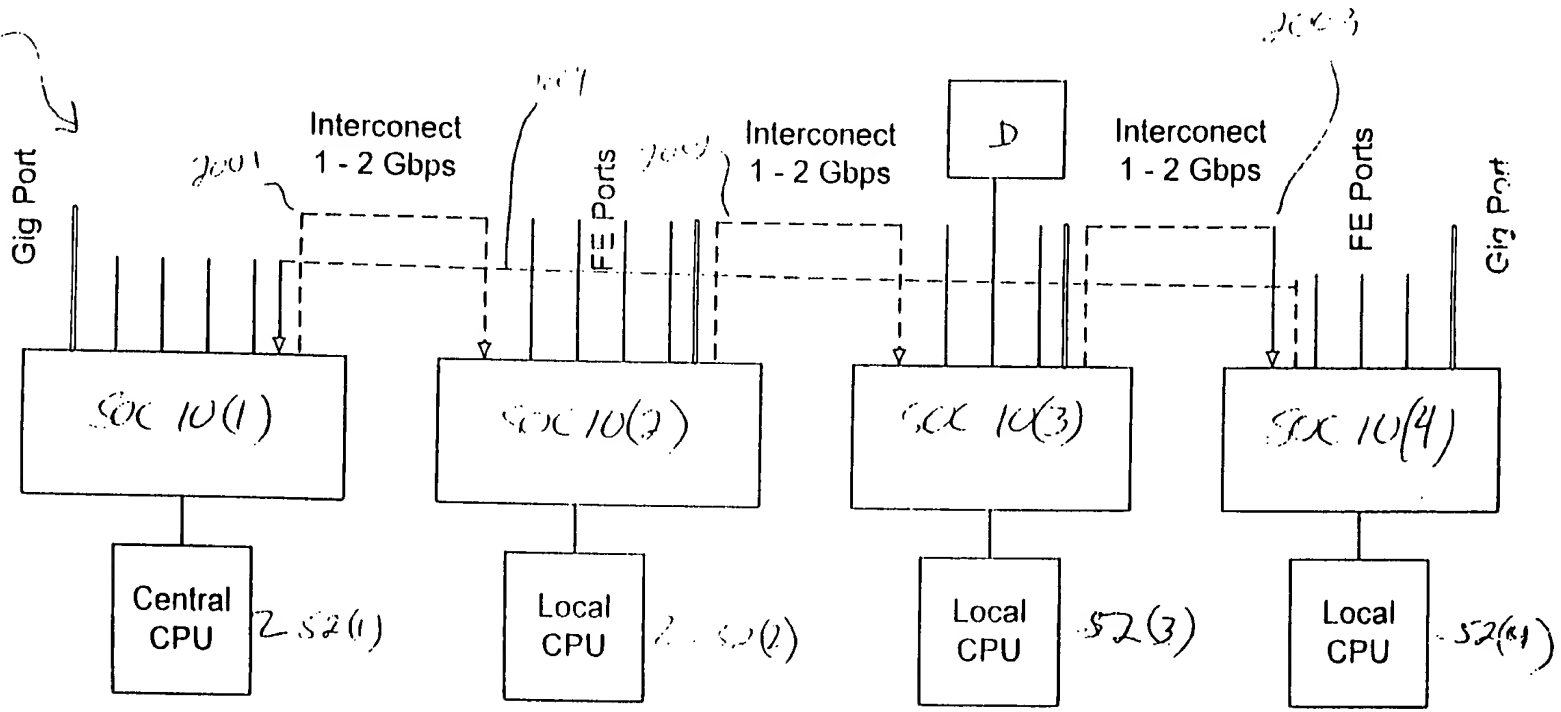

Gig Port
Interconect
1 - 2 Gbps
FE Ports
Interconect
1 - 2 Gbps
Interconect
1 - 2 Gbps
FE Ports
Gig Port
SIC 10(1)
SIC 10(2)
SIC 10(3)
SIC 10(4)
Central
CPU
Local
CPU
Local
CPU
Local
CPU

Fig 29

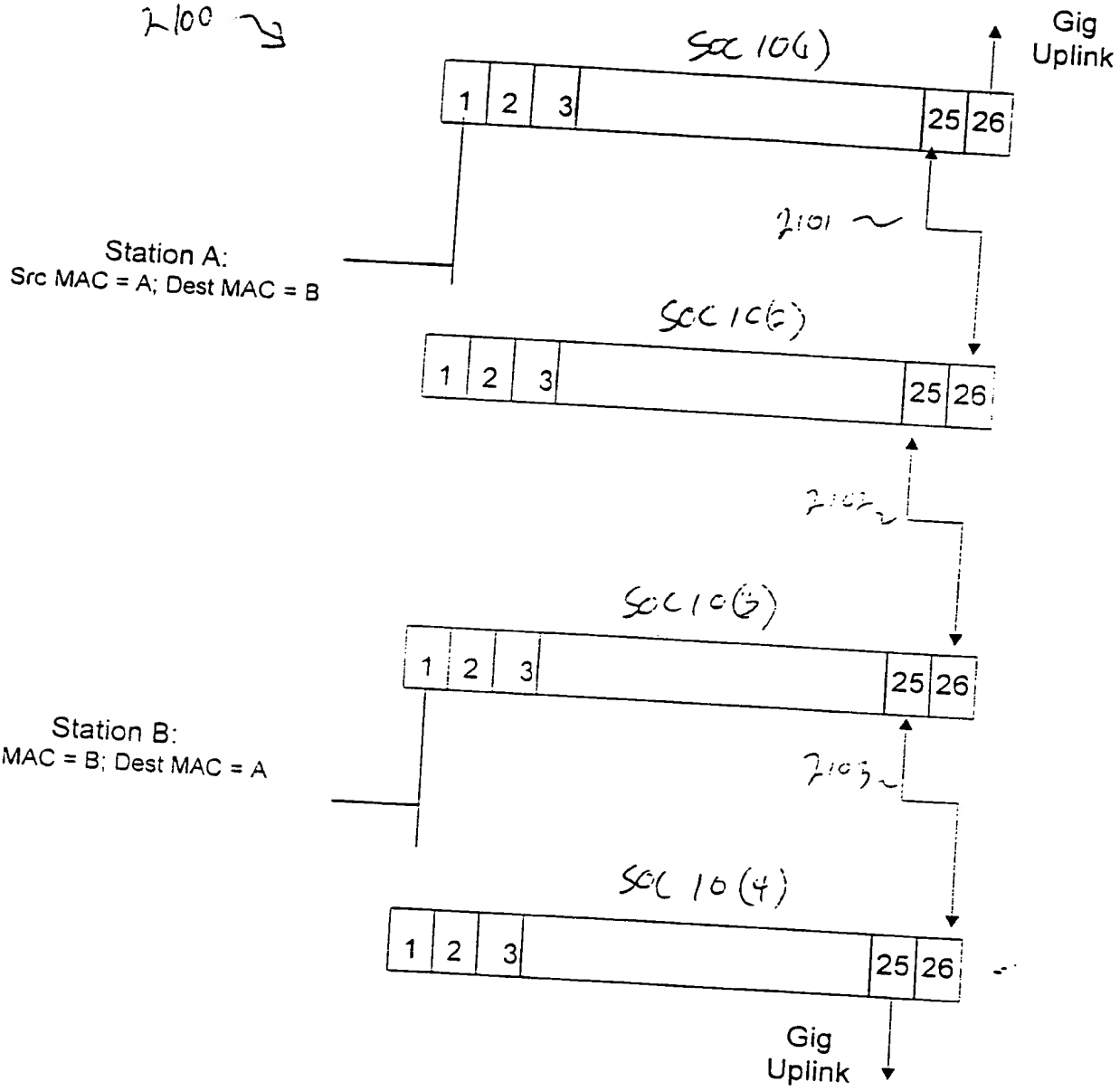

2100
SOC 10(6)
Gig Uplink
1
2
3
25
26
2101
Station A:
Src MAC = A; Dest MAC = B
SOC 10(2)
2102
SOC 10(3)
Station B:
Src MAC = B; Dest MAC = A
2103
SOC 10(4)
Gig Uplink

Fig. 30

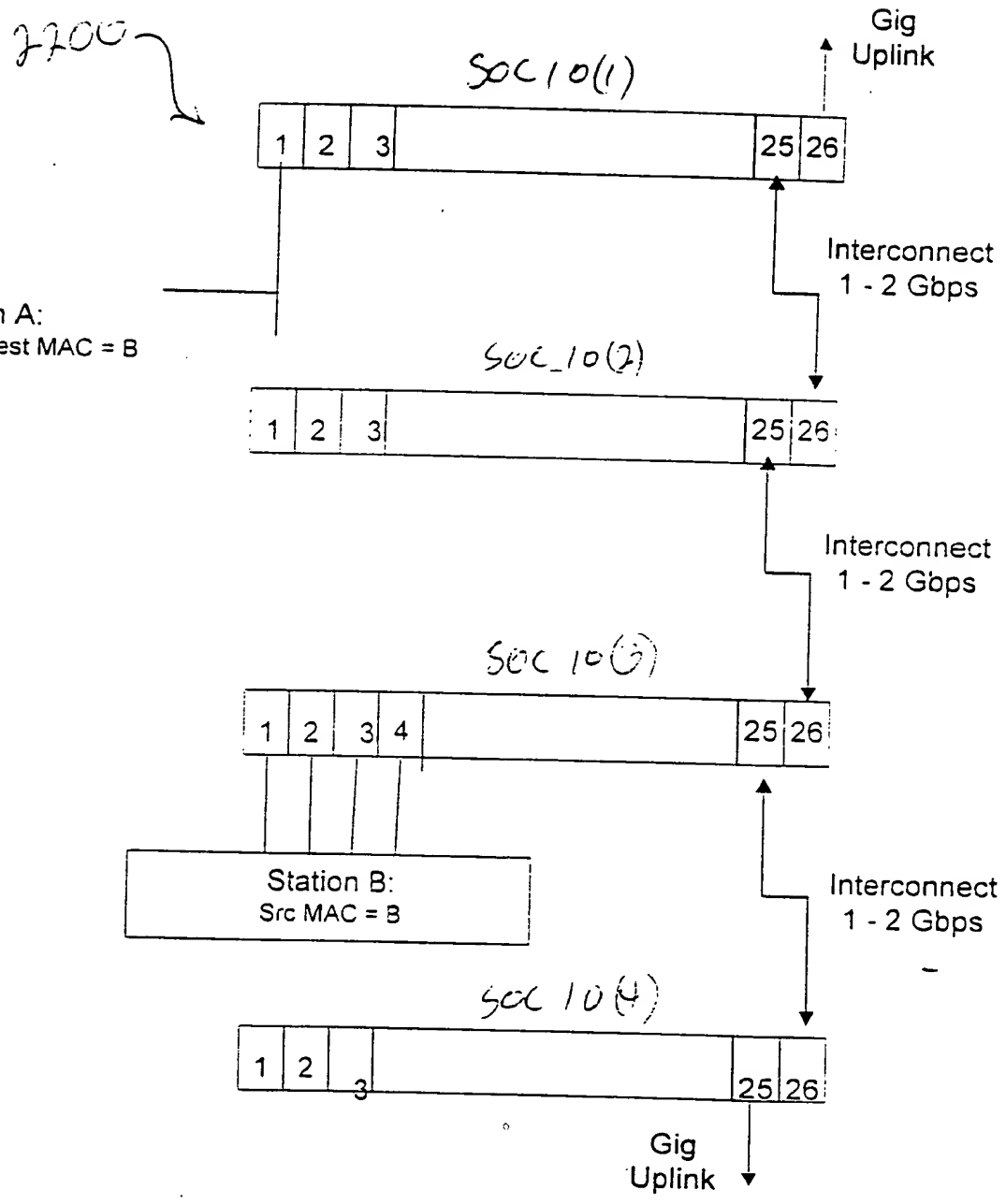

3200
SOC 10(1)
Gig Uplink
1
2
3
25
26
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
SOC_10(2)
1
2
3
25
26
Interconnect 1 - 2 Gbps
SOC 10(3)
1
2
3
4
25
26
Station B:
Src MAC = B
Interconnect 1 - 2 Gbps
SOC 10(4)
1
2
3
25
26
Gig Uplink

Fig 31

Fig 32A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	0	X	X
25	B	1	1	2	2

Fig 32B

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
25	B	1	1	2	2

Fig 32C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig 32D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X

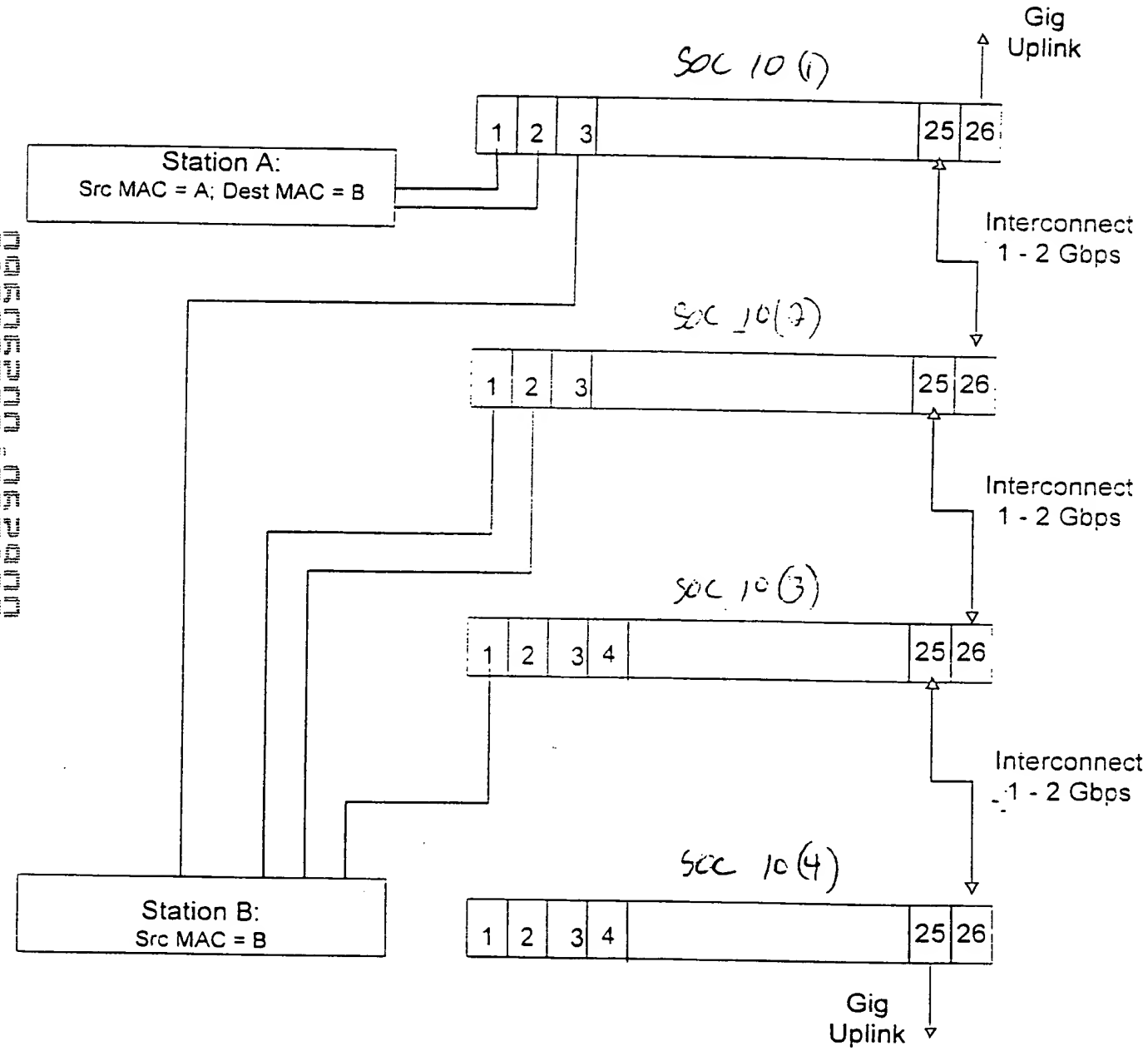

Gig
Uplink
SOC 10 (1)
1
2
3
25
26
Station A:
Src MAC = A; Dest MAC = B
Interconnect
1 - 2 Gbps
SOC 10(2)
1
2
3
25
26
Interconnect
1 - 2 Gbps
SOC 10(3)
1
2
3
4
25
26
Interconnect
1 - 2 Gbps
SOC 10(4)
Station B:
Src MAC = B
1
2
3
4
25
26
Gig
Uplink

Fig 33

Fig. 34A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	1	1	1
25	B	1	1	2	2

Fig. 34B

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1
25	B	1	1	2	2

Fig. 34C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1
1	B	1	1	2	2

Fig. 34D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1

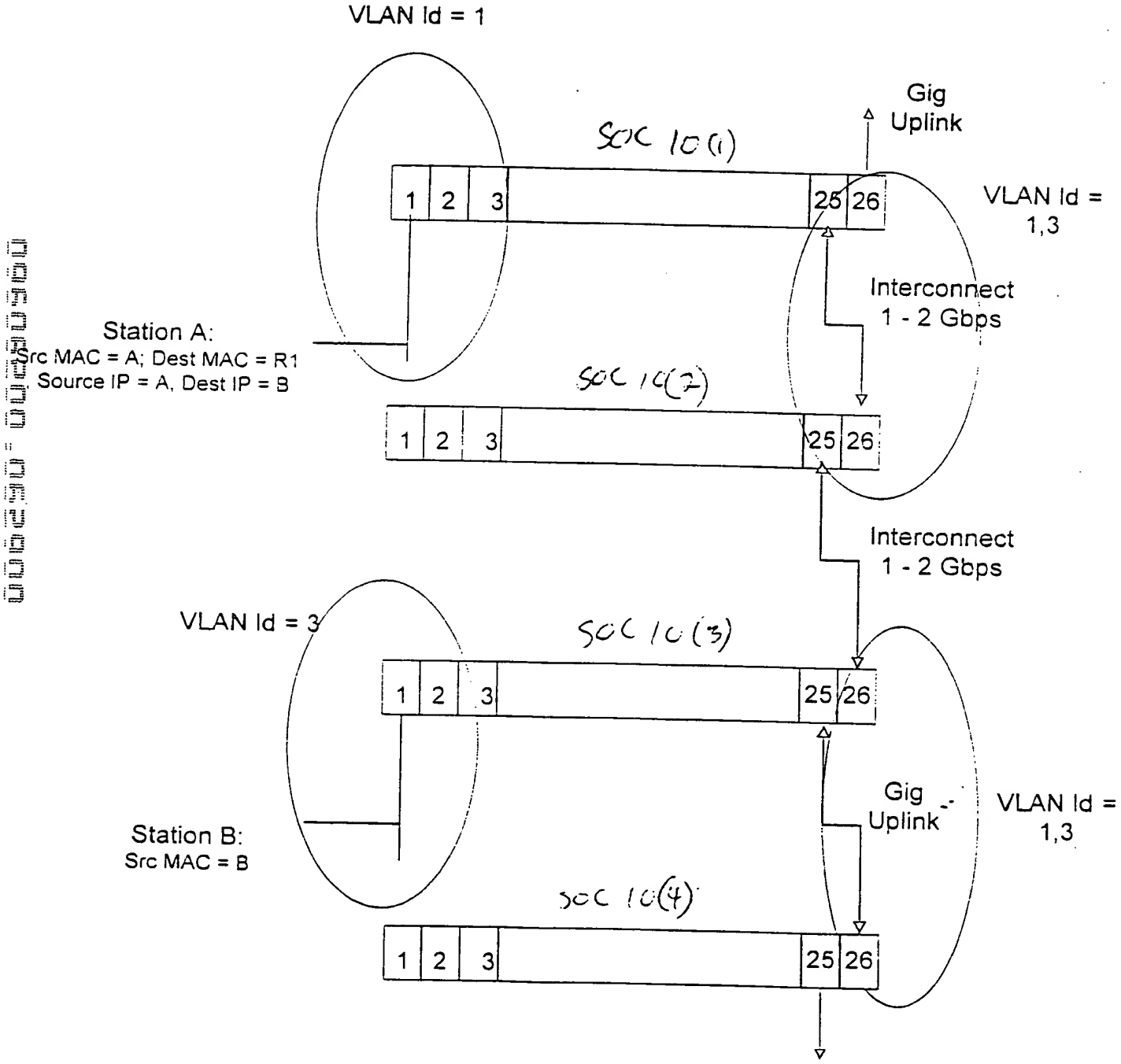

VLAN Id = 1
Gig Uplink
SOC 10(1)
1 2 3
25 26
VLAN Id = 1,3
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = R1
Source IP = A, Dest IP = B
SOC 10(2)
1 2 3
25 26
Interconnect 1 - 2 Gbps
VLAN Id = 3
SOC 10(3)
1 2 3
25 26
Gig Uplink
VLAN Id = 1,3
Station B:
Src MAC = B
SOC 10(4)
1 2 3
25 26

Fig. 35

Trunk Group Table for SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	25	25	25	25	X	X	X	X	4

Trunk Group Table for SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	25	25	25	25	X	X	X	X	4

Trunk Group Table for SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	1	2	3	4	X	X	X	X	4

Trunk Group Table for SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	26	26	26	26	X	X	X	X	4

Fig. 36

Trunk Group Table for SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	1	2	X	X	X	X	X	X	2
2	25	25	25	3	X	X	X	X	4

Trunk Group Table for SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	25	1	2	26	X	X	X	X	4

Trunk Group Table for SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	1	26	26	26	X	X	X	X	4

Trunk Group Table for SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	26	26	26	26	X	X	X	X	4

Fig. 37

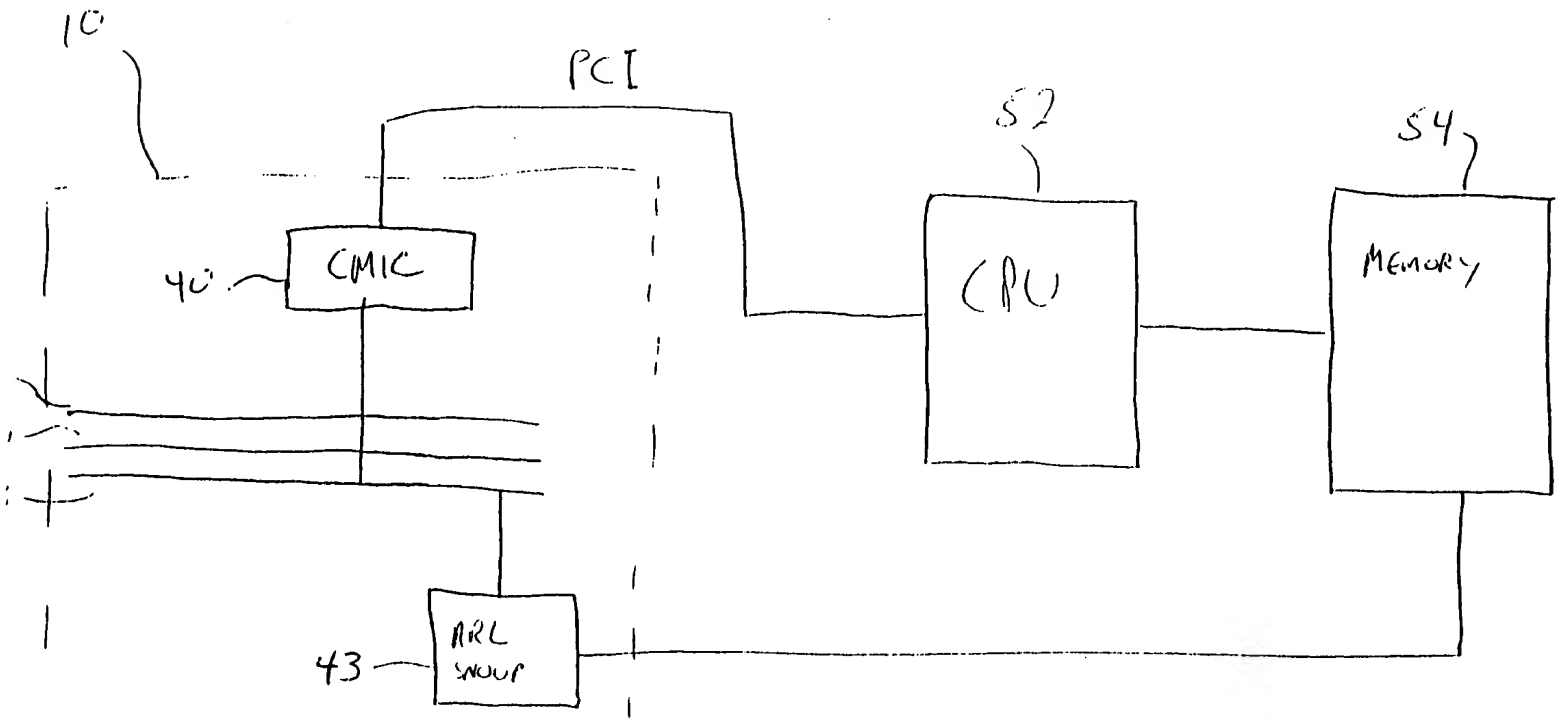


Fig. 3B

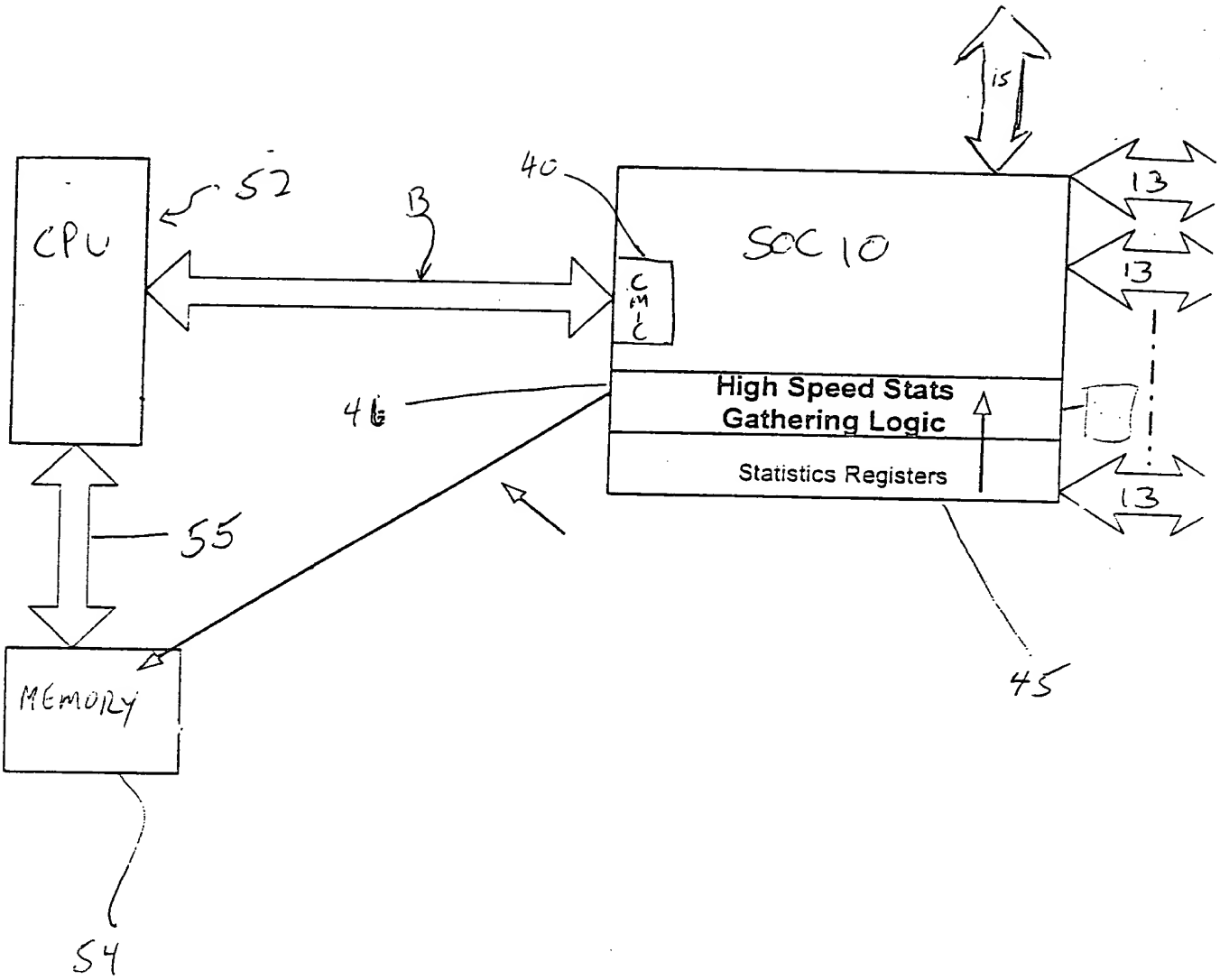

CPU
52
B
40
SOC 10
CMIC
15
13
13
13
46
High Speed Stats
Gathering Logic
Statistics Registers
55
MEMORY
45
54

Fig. 39

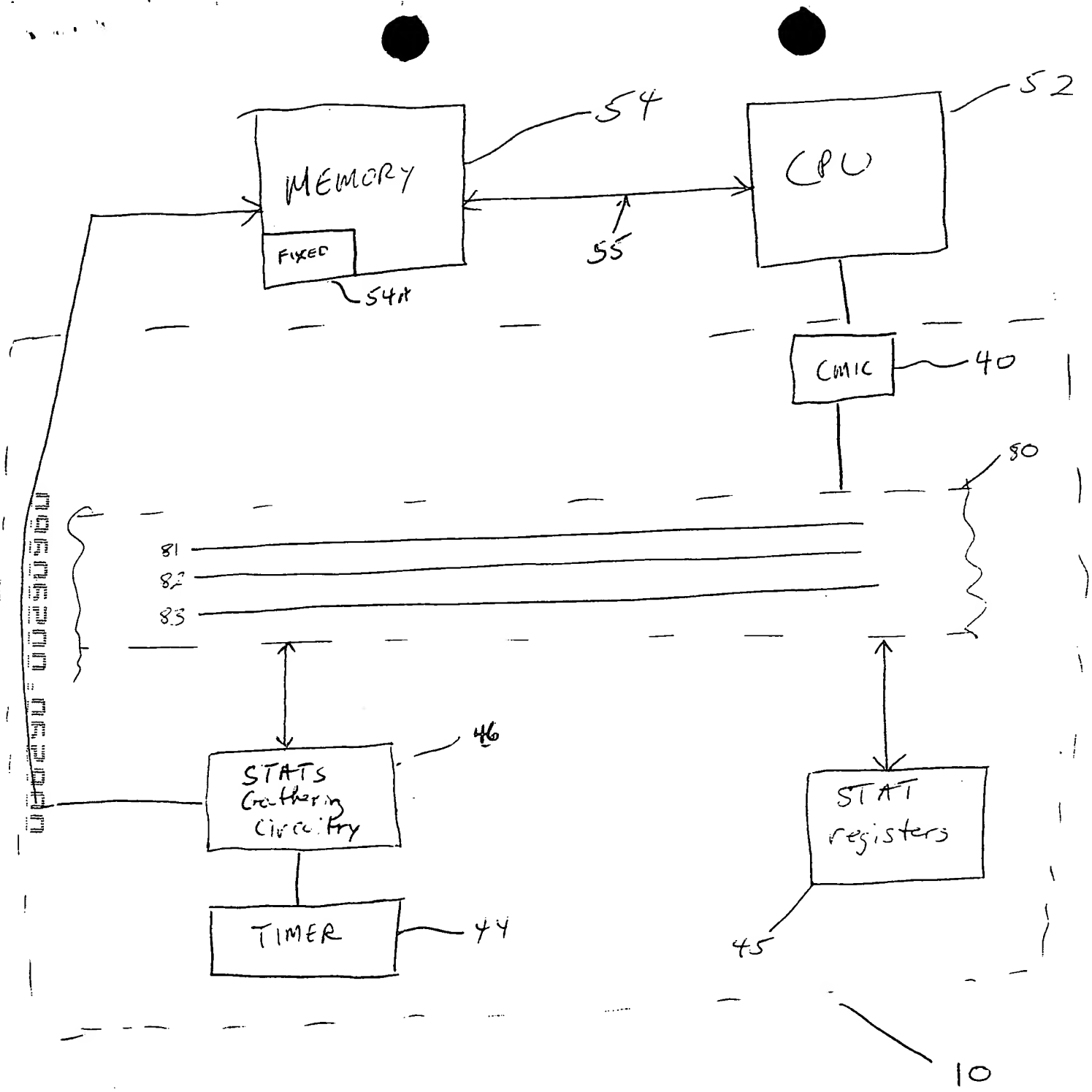

MEMORY
54
FIXED
54A
55
CPU
52
CMIC
40
80
81
82
83
STATS Gathering Circuitry
46
TIMER
44
STAT registers
45
10

Fig. 40

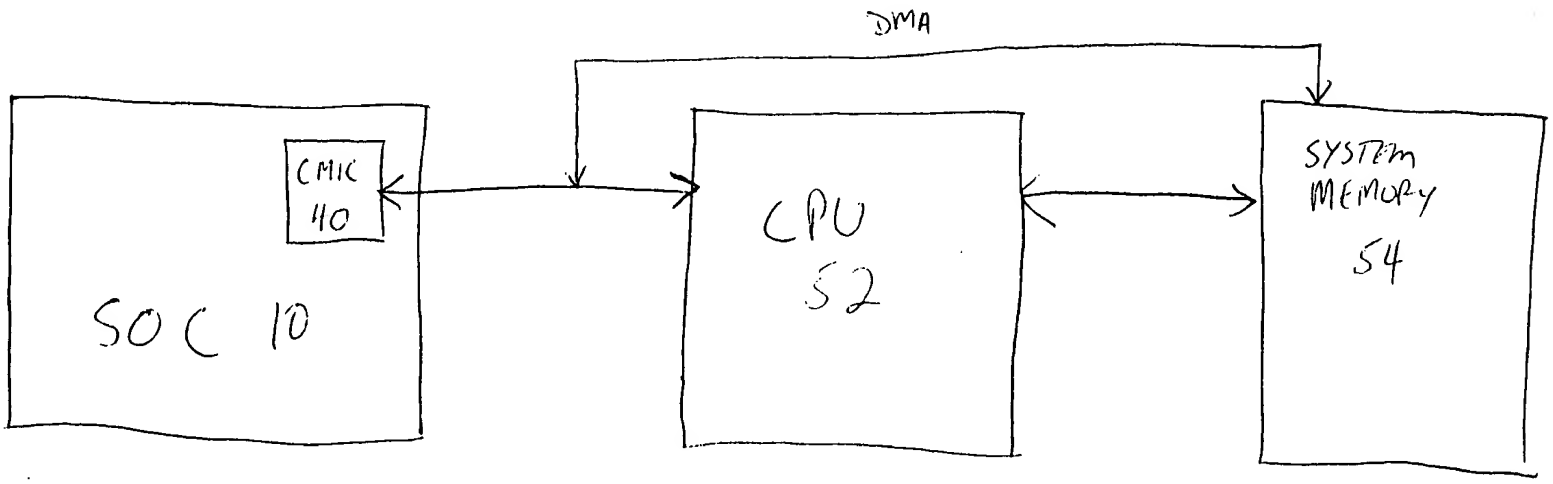


Fig. 4

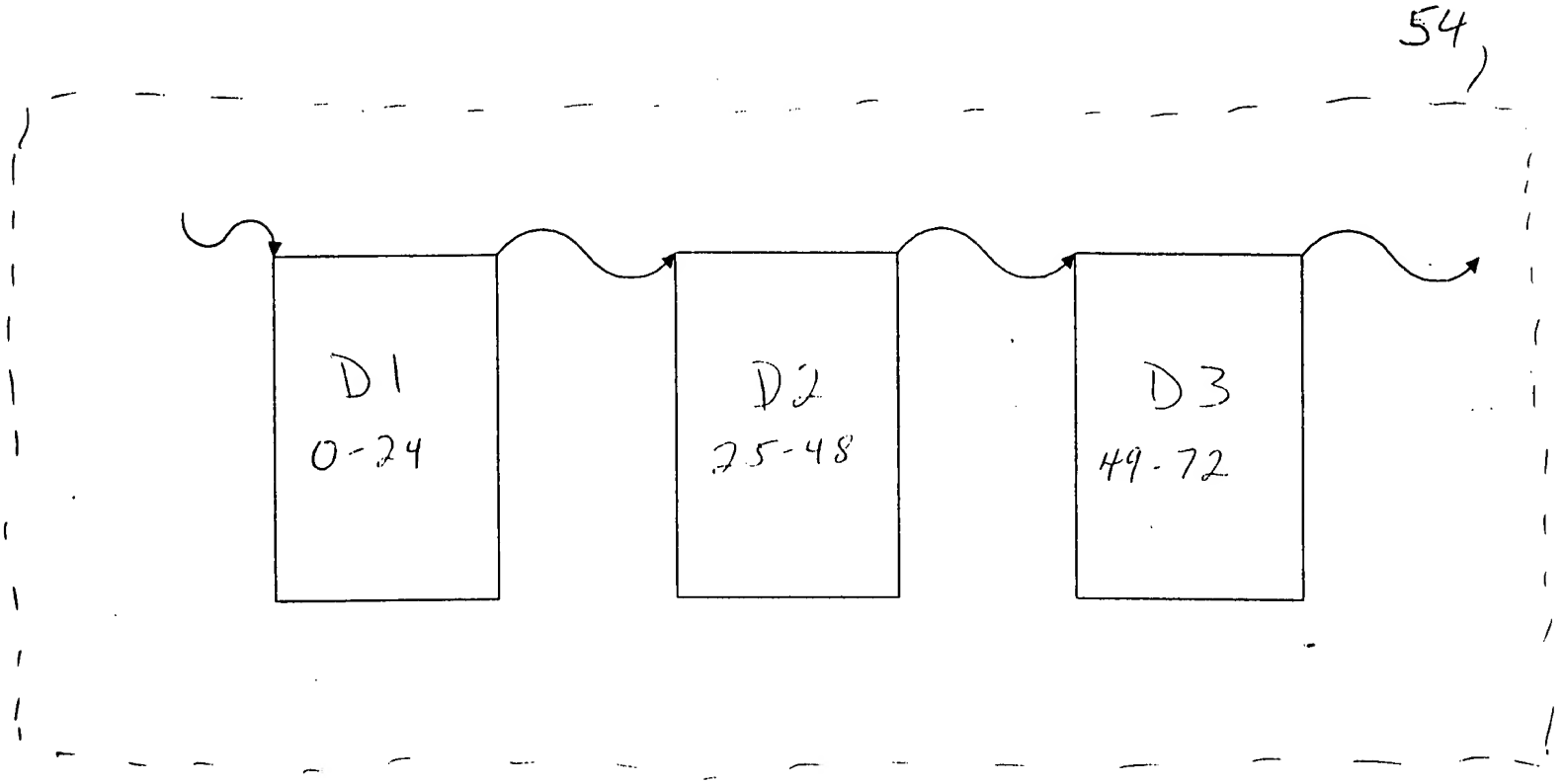


Fig. 42

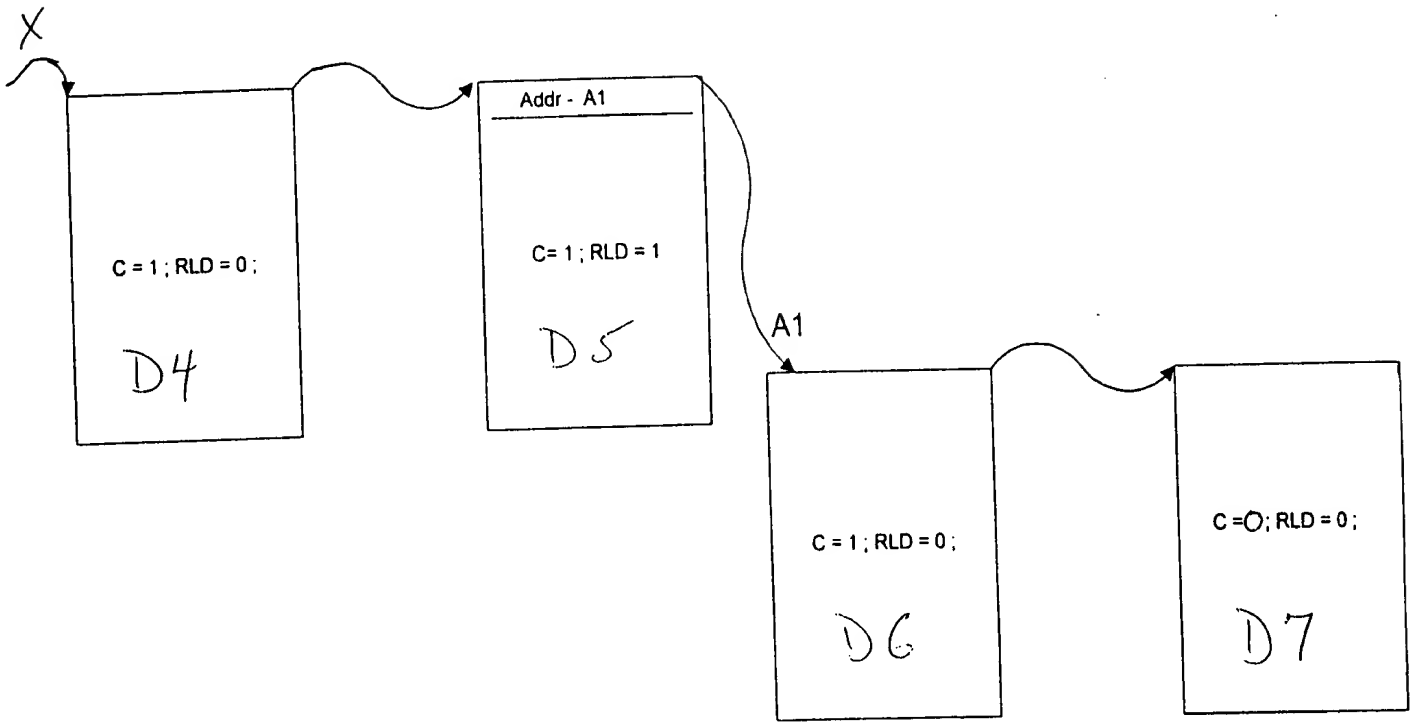


Fig. 43